Project Name : F71IXX

Platform : Montevina Penryn(CPU)+Cantiga(NB)+ICH9M(SB)+NB9P/M

PAGE CONTENT

Schematic Version Change History

Release Date	Version	PCB P/N	PCBA P/N	Note
2007/10/19	Rev.A	37GF50000-A0	82GF50000-A0	Initial
2007/12/21	Rev.B	37GF50000-B0	82GF50000-B0	UPDATE
2008/3/7	Rev.C	37GF50000-C0	82GF50000-C0	UPDATE

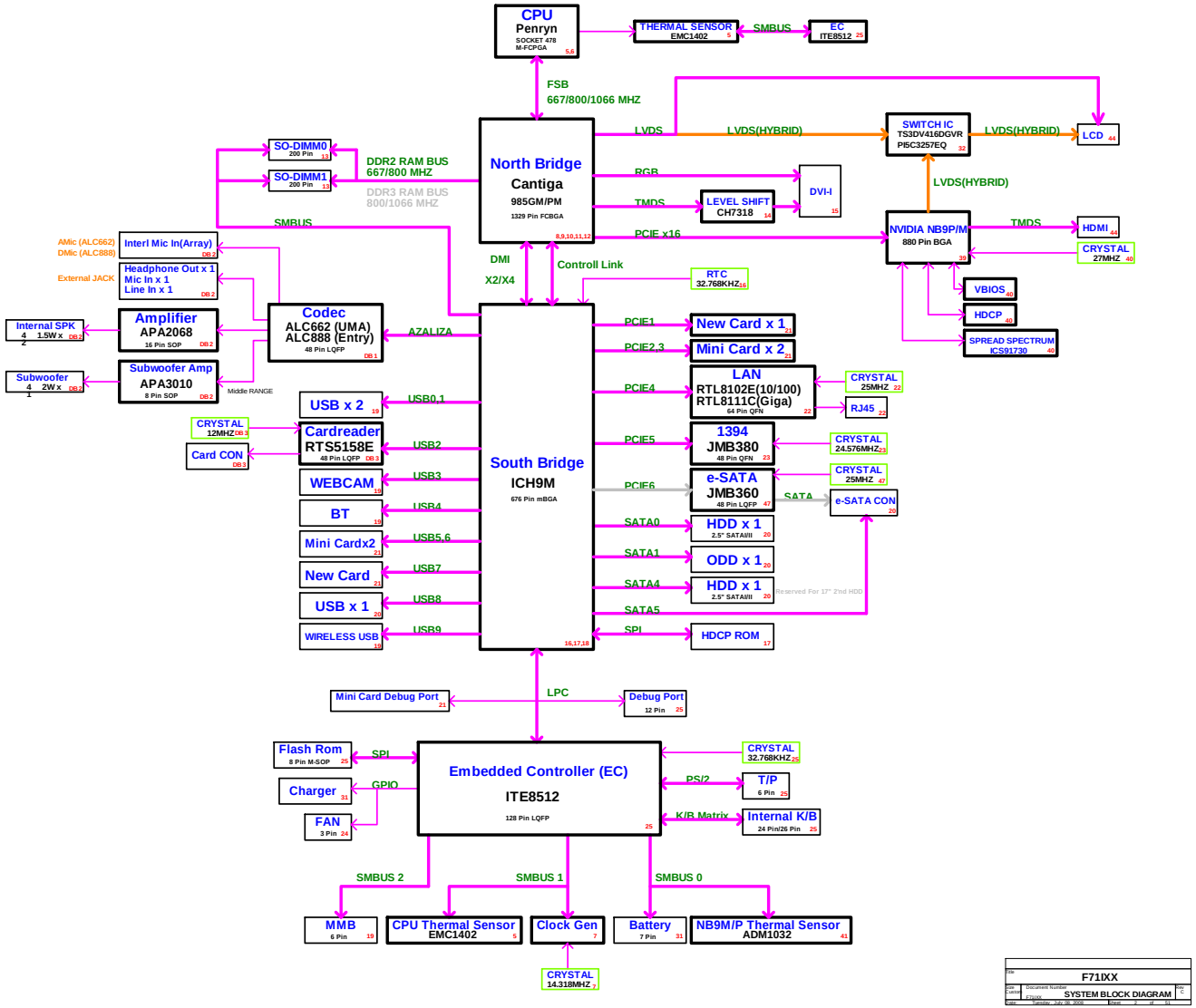
Component Identify Color By Project

- F50II0 only
- F50IN0 only
- F50IN5 only
- F50II0/F50IN5
- F50II0/IN0
- F50IN0/IN5
- Depend on project (check table)
- Reserved (verify at A phase)
- All project

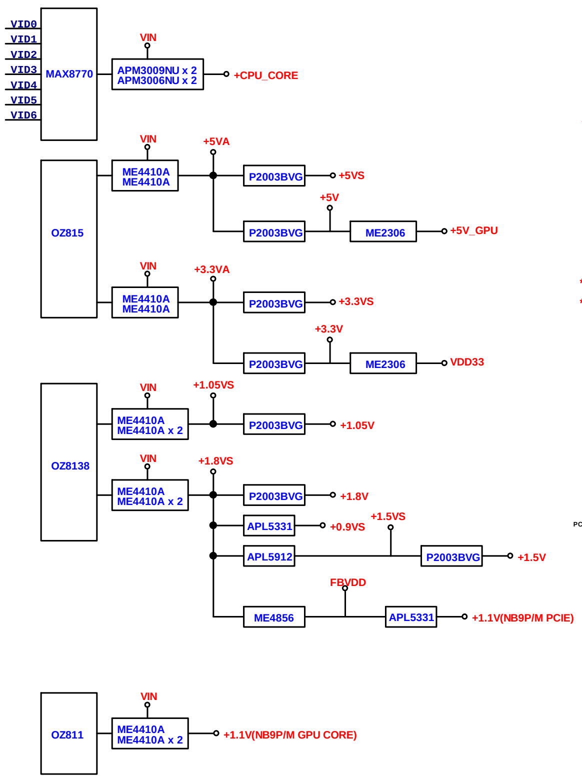
SMT Process Identify Mark

* DIP component

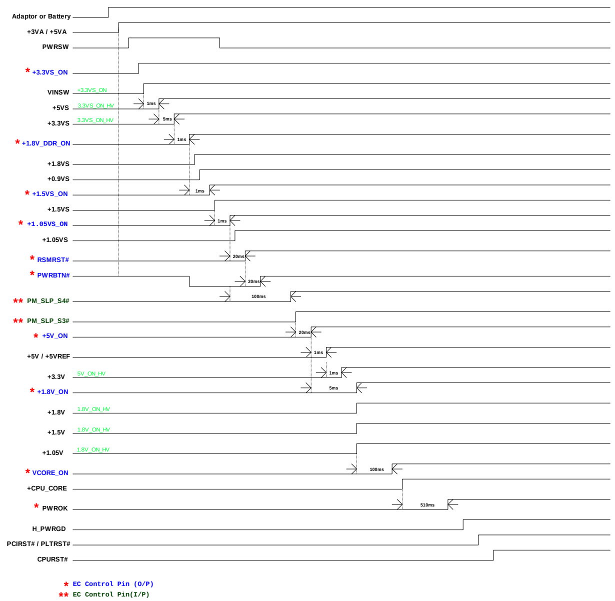
Title	F71IXX	
Size: Custom	Document Number: F71IXX — INDEX	Rev: C
Date: Tuesday, July 08, 2008	Sheet 1 of 51	


CPU
Penryn
SOCKET 478
M-FCPGA
THERMAL SENSOR
EMC1402
SMBUS
EC
ITE8512
FSB
667/800/1066 MHZ
North Bridge
Cantiga
985GM/PM
1329 Pin FCBGA
LVDS
LVDS(HYBRID)
SWITCH IC
TS3DV416DGVR
PI5C3257EQ
LCD
RGB
DVI-I
TMDS
LEVEL SHIFT
CH7318
PCIE x16
NVIDIA NB9P/M
880 Pin BGA
HDMI
CRYSTAL
27MHZ
VBIOS
HDCP
SPREAD SPECTRUM
ICS91730
SO-DIMM0
SO-DIMM1
DDR2 RAM BUS
667/800 MHZ
DDR3 RAM BUS
800/1066 MHZ
SMBUS
DMI
X2/X4
Controll Link
RTC
32.768KHZ
AMic (ALC662)
DMic (ALC888)
Interl Mic In(Array)
External JACK
Headphone Out x 1
Mic In x 1
Line In x 1
Amplifier
APA2068
16 Pin SOP
Internal SPK
4 1.5W x 2
Subwoofer
4 2W x 1
Subwoofer Amp
APA3010
8 Pin SOP
Middle RANGE
Codec
ALC662 (UMA)
ALC888 (Entry)
48 Pin LQFP
AZALIZA
South Bridge
ICH9M
676 Pin mBGA
PCIE1
New Card x 1
PCIE2,3
Mini Card x 2
PCIE4
LAN
RTL8102E(10/100)
RTL8111C(Giga)
64 Pin QFN
RJ45
PCIE5
1394
JMB380
48 Pin QFN
PCIE6
e-SATA
JMB360
48 Pin LQFP
SATA
e-SATA CON
SATA0
HDD x 1
2.5" SATAIII
SATA1
ODD x 1
SATA4
HDD x 1
2.5" SATAIII
Reserved For 17" 2'nd HDD
SATA5
SPI
HDCP ROM
USB x 2
USB0,1
CRYSTAL
12MHZ
Cardreader
RTS5158E
48 Pin LQFP
Card CON
USB2
WEBCAM
USB3
BT
USB4
Mini Cardx2
USB5,6
New Card
USB7
USB x 1
USB8
WIRELESS USB
USB9
Mini Card Debug Port
LPC
Debug Port
12 Pin
Flash Rom
8 Pin M-SOP
SPI
Charger
GPIO
FAN
3 Pin
Embedded Controller (EC)
ITE8512
128 Pin LQFP
CRYSTAL
32.768KHZ
PS/2
T/P
6 Pin
K/B Matrix
Internal K/B
24 Pin/26 Pin
SMBUS 2
SMBUS 1
SMBUS 0
MMB
6 Pin
CPU Thermal Sensor
EMC1402
Clock Gen
Battery
7 Pin
NB9M/P Thermal Sensor
ADM1032
CRYSTAL
14.318MHZ
F71IXX
SYSTEM BLOCK DIAGRAM

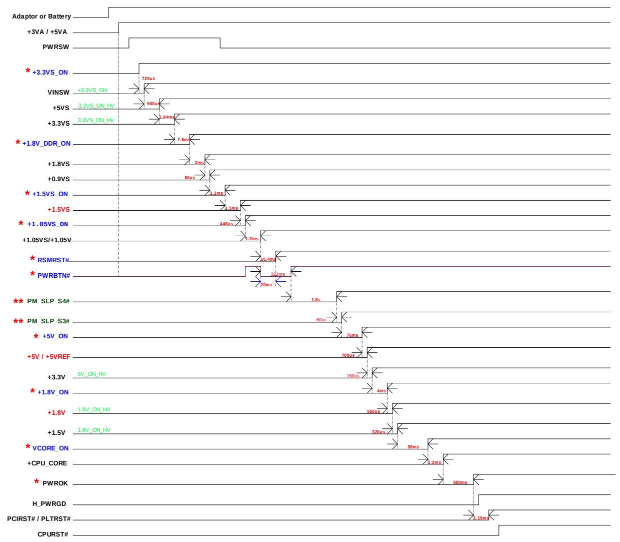
POWER BLOCK DIAGRAM



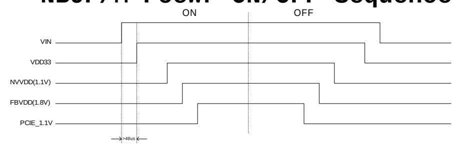
System Poewr On Sequence (spec)



F50IN0 Power On Sequence B phase(real)



NB9P/M Poewr ON/OFF Sequence



Title	F71IXX
Document Number	POWER DIAGRAM & SEQUENCE

ICH9M GPIO	
GPIO0	PM_BM_BUSY#
GPIO1	EC_EXTSMI#
GPIO2	INT_PIRQE#
GPIO3	INT_PIRQF#
GPIO4	INT_PIRQG#
GPIO5	INT_PIRQH#
GPIO6	BIOS_REC
GPIO7	***N.C***(TACH3)
GPIO8	***N.C***
GPIO9	***N.C***(WOL_EN)
GPIO10	***N.C***(ALERT#)
GPIO11	SMB_ALERT#
GPIO12	LAN_PHYPC
GPIO13	***N.C***(GLAN_DOCK#)
GPIO14	***N.C***(NETDETECT)
GPIO15	PM_STPPCI#
GPIO17	***N.C***(TACH0)
GPIO18	***N.C***
GPIO19	SATA1GP
GPIO21	SATA0GP
GPIO22	***N.C***(SCLOCK)
GPIO23	LDRQ1#
GPIO24	CRB_SV_DET
GPIO25	PM_STPCPU#
GPIO26	PM_SLP_S4_STATE#
GPIO27	QRT_STATE0
GPIO28	QRT_STATE1
GPIO29	USB_OC#5
GPIO30	USB_OC#6
GPIO31	USB_OC#7
GPIO32	PM_CLKRUN#
GPIO33	HDA_DOCK_EN
GPIO34	***N.C***(HDA_DOCK_RST)
GPIO35	CLK_SATA_OE#
GPIO36	SATA2GP
GPIO37	SATA3GP
GPIO38	ODD_DET
GPIO39	ICH_GPIO39
GPIO40	USB_OC#1
GPIO41	USB_OC#2
GPIO42	USB_OC#3
GPIO43	USB_OC#4
GPIO48	MFG_MODE
GPIO49	H_PWRGD
GPIO50	PCI_REQ#1
GPIO51	PCI_GNT#1
GPIO52	PCI_REQ#2
GPIO53	PCI_GNT#2
GPIO54	PCI_REQ#3
GPIO55	PCI_GNT#3

ITE8512E GPIO	
GPA0	PM_RSMRST#
GPA1	SUSPEND_LED
GPA2	SILENT_LED
GPA3	RF_LED
GPA4	CAPS_LED
GPA5	NUM_LED
GPA6	SCROLL/3G_LED
GPA7	EXTTS#0
GPB0	PM_SLP_S4#
GPB1	PM_SLP_S3#
GPB2	CMI_TX
GPB3	SMB_CLK0
GPB4	SMB_DAT0
GPB5	H_A20GATE
GPB6	H_RCIN#
GPB7	QRT_STATE
GPC0	CMI_RX
GPC1	SMB_CLK1
GPC2	SMB_DAT1
GPC3	KEY_OUT16
GPC4	RF_SW#
GPC5	KEY_OUT17
GPC6	BTL_BEEP
GPC7	SILENT#
GPD0	EC_PREST#
GPD1	PWRBTN#
GPD2	MUTE
GPD3	EC_EXTSMI#
GPD4	***N.C***
GPD5	SMP1_EN#
GPD6	CHG_ON
GPD7	LCDSW
GPE0	PWRSW
GPE1	SET_V
GPE2	PWROK
GPE3	BT_ON
GPE4	LID#
GPE5	CPPE#
GPE6	FAN_SPD#
GPE7	PCI_RST#
GPF0	EC_CPU_200MHz
GPF1	***N.C***
GPF2	CHG_G_LED
GPF3	CHG_R_LED
GPF4	TP_CLK
GPF5	TP_DATA
GPF6	***N.C***
GPF7	***N.C***
GPG0	SB_RTCRST
GPG1	EC_WDOG OK
GPG2	FLFRAME#
GPG6	MPWORK
GPH0	+1.8V_ON
GPH1	+1.8V_DDR_ON
GPH2	VCORE_ON
GPH3	+3.3VS_ON
GPH4	+5V_ON
GPH5	+1.05VS_ON
GPH6	+1.5VS_ON

ITE8512E GPIO	
GPI0	BATT_TEMP
GPI1	ADAPTOR_I
GPI2	ADAP_IN
GPI3	BAT_CHG_I
GPI4	BAT_I
GPI5	***CPU_PWR***
GPI6	DDR2_TEMP
GPI7	VGA_TEMP
GPJ0	EC_BRGHT
GPJ1	CHG_I
GPJ2	FAN_CTRL0
GPJ3	BROWSER#
GPJ4	MAIL#
GPJ5	PM_THROTTING#

Penryn CPU

	CPU CORE(V)	ICC(A)	W	TEMP( )
IMVP-6+	1.25	44.0	46.2	

Cantiga

VCC	ICC(mA)	W	TEMP( )
+3.3V	262	0.87	105
+1.8VS	3178	5.73	
+1.5V	86	0.129	
+1.05	14688.52	15.43	

ICH9M

VCC	ICC(mA)	mW	TEMP( )
+5V	2	10	70
+5VS	2	10	
+3.3V	347	1145.1	
+3.3VS	212	699.6	
+1.5V	1988	2982	
+1.05V	1634	1715.7	

ITE8512E

VCC	ICC(mA)	mW	TEMP( )
+3.3V	100	330	70

CLOCK GENERATOR ICS9LPR365

VCC	ICC(mA)	mW	TEMP( )
+3.3V	250	825	70

ALC888

VCC	ICC(mA)	mW	TEMP( )
+3.3V(DVDD)	40	132	70
+5V(AVDD)	51	255	

APA2068

VCC	ICC(mA)	mW	TEMP( )
+5V	20	100	85

ADM1032

VCC	ICC	mW	TEMP( )
+3.3V	170uA	0.56	150

RTL8111C

VCC	ICC(mA)	mW	TEMP( )
+3.3VS	103	339.9	70
+1.8VS	198	356.4	
+1.5VS	367	550.5	

JMB360

VCC	ICC(mA)	mW	TEMP( )
+3.3V	TBD		70
+1.8V	TBD		

Title: **F71IXX**

Size: Custom | Document Number: F71IXX | **GPIO & Power Consumption** | Rev: C

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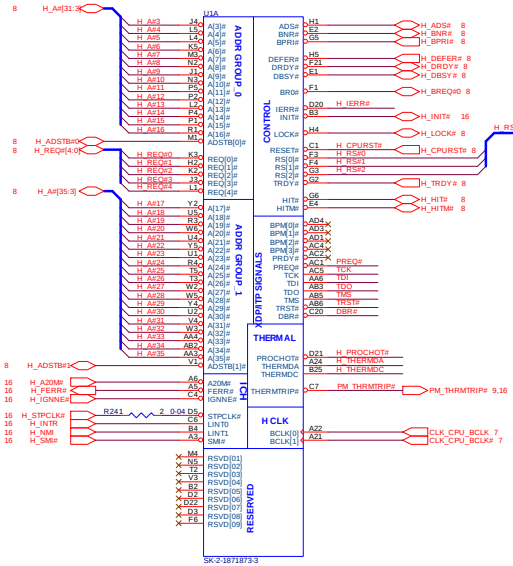
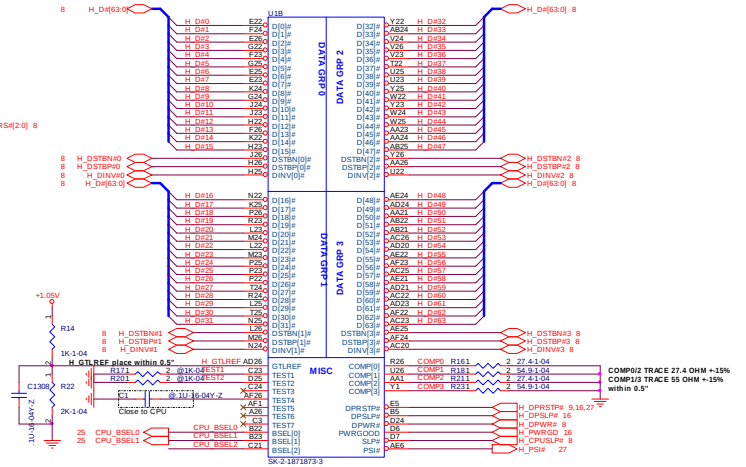
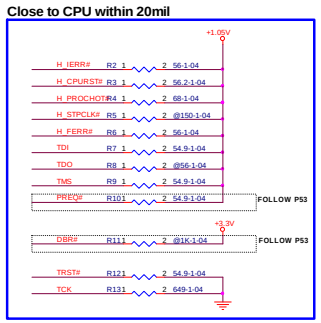
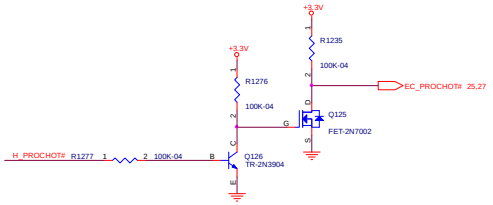
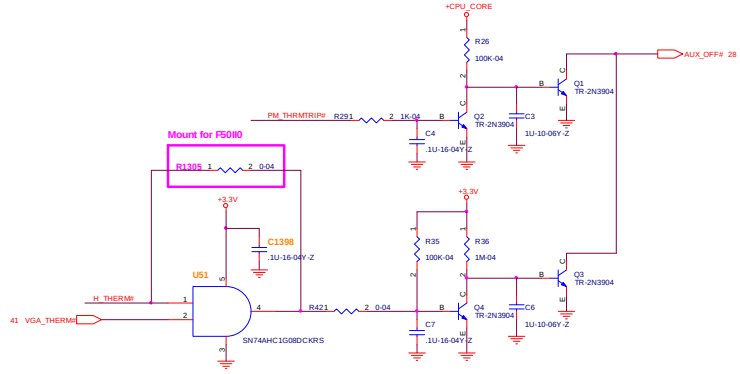






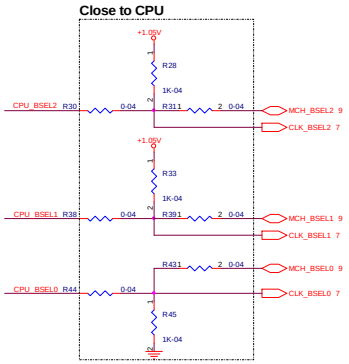
FSB \ BSEL	BSEL2	BSEL1	BSEL0	MHZ
FSB667	0	1	1	166
FSB800	0	1	0	200
FSB1066	0	0	0	266

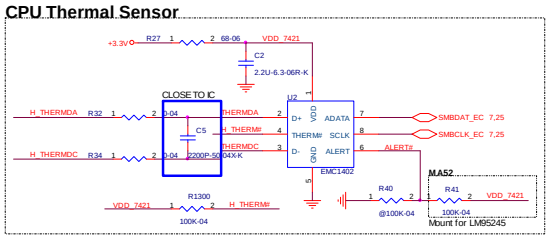




Input		Output
PIN1	PIN2	PIN4
H	H	H
L	X	L
X	L	L

	F50II0	F50IN0	F50IN5
R1305	mount	option	
U51	option	mount	





IC \ SETTING	R32	R34	R41
EMC1402	0R	0R	@100K
ADT7421	100R_1	100R_1	@100K
LM95245	0R	0R	100K

Title	F71IXX
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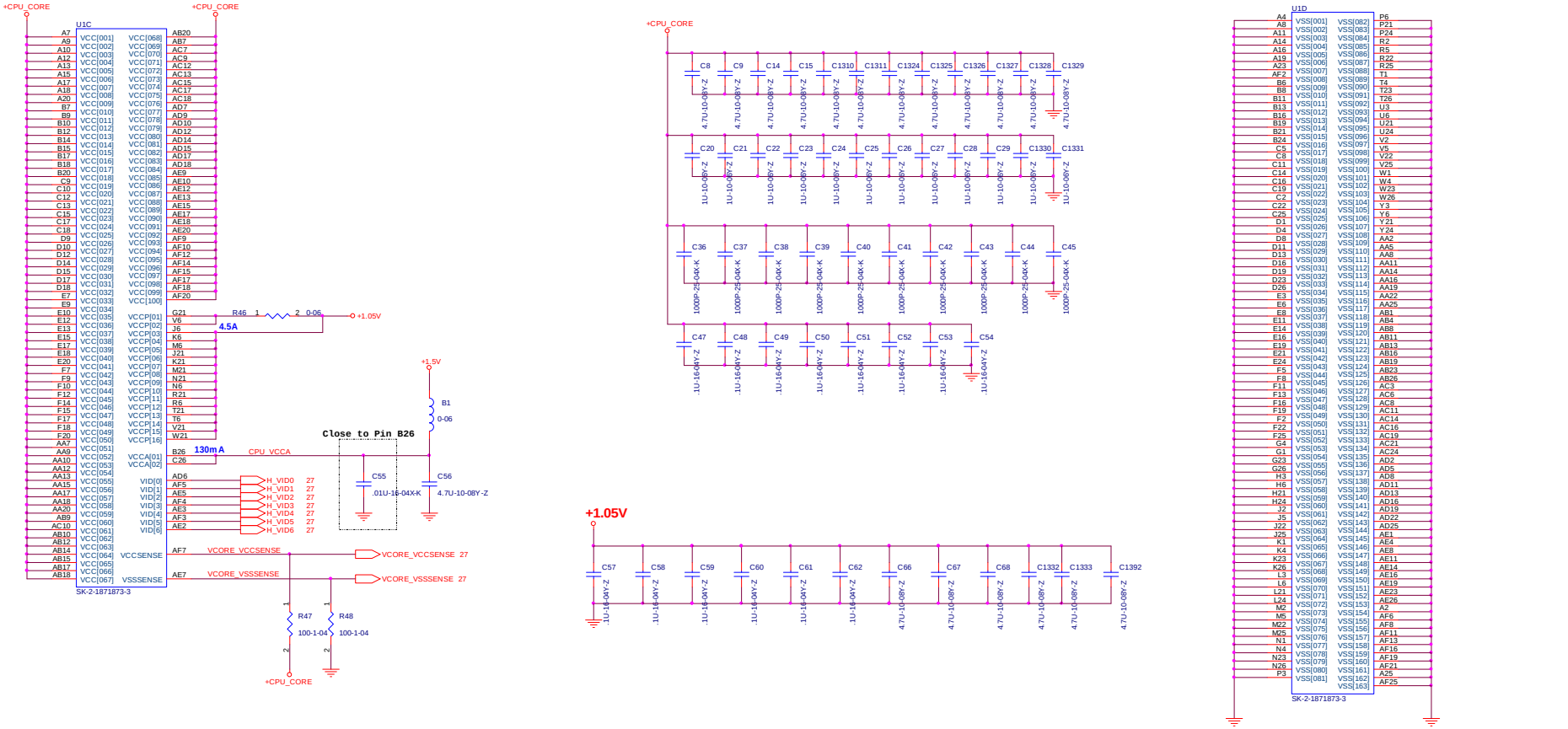

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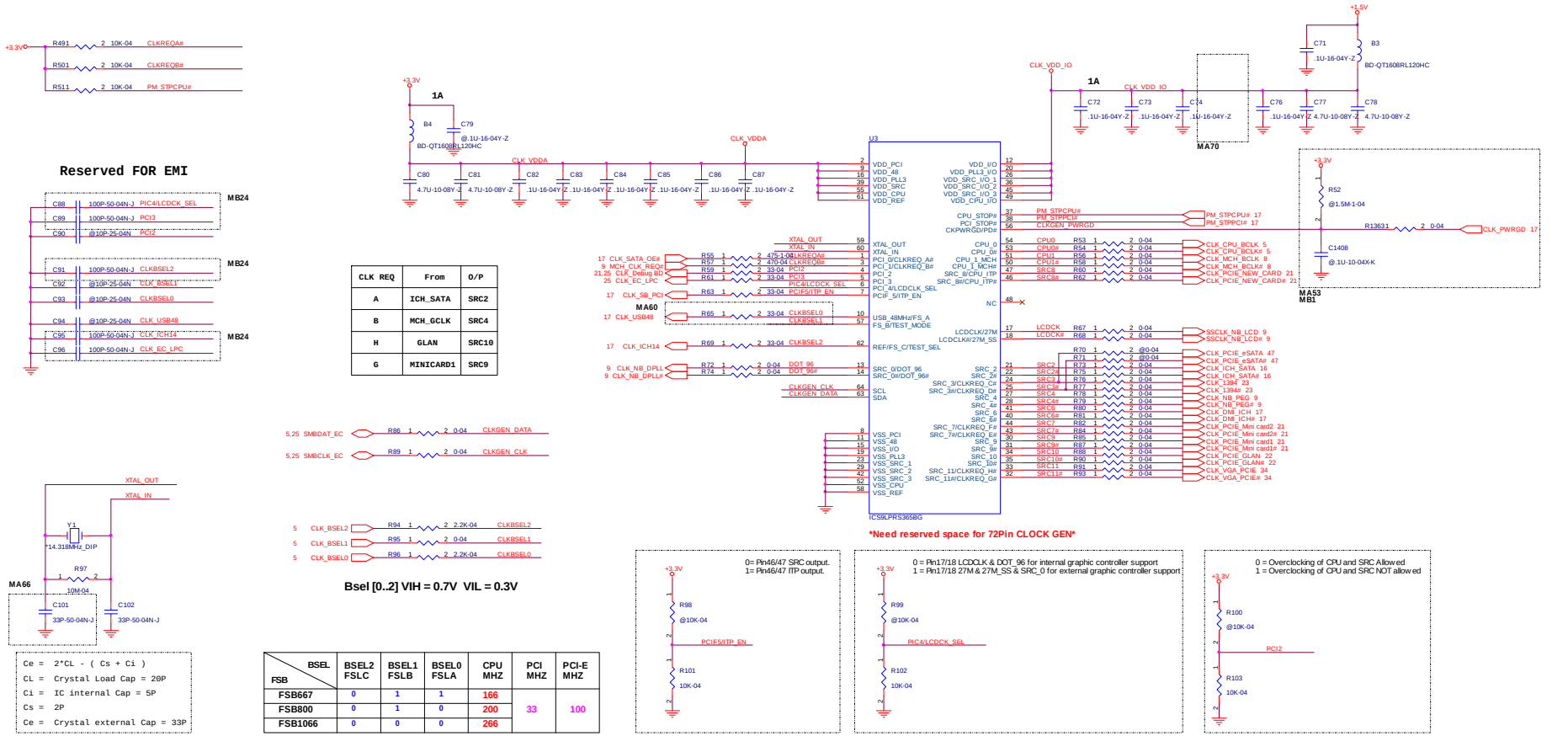

CLK_REQ	From	O/P
A	ICH_SATA	SRC2
B	MCH_GCLK	SRC4
H	GLAN	SRC10
G	MINICARD1	SRC9

FSB \ BSEL	BSEL2 FSLC	BSEL1 FSLB	BSEL0 FSLA	CPU MHZ	PCI MHZ	PCI-E MHZ
FSB667	0	1	1	166	33	100
FSB800	0	1	0	200		
FSB1066	0	0	0	266		

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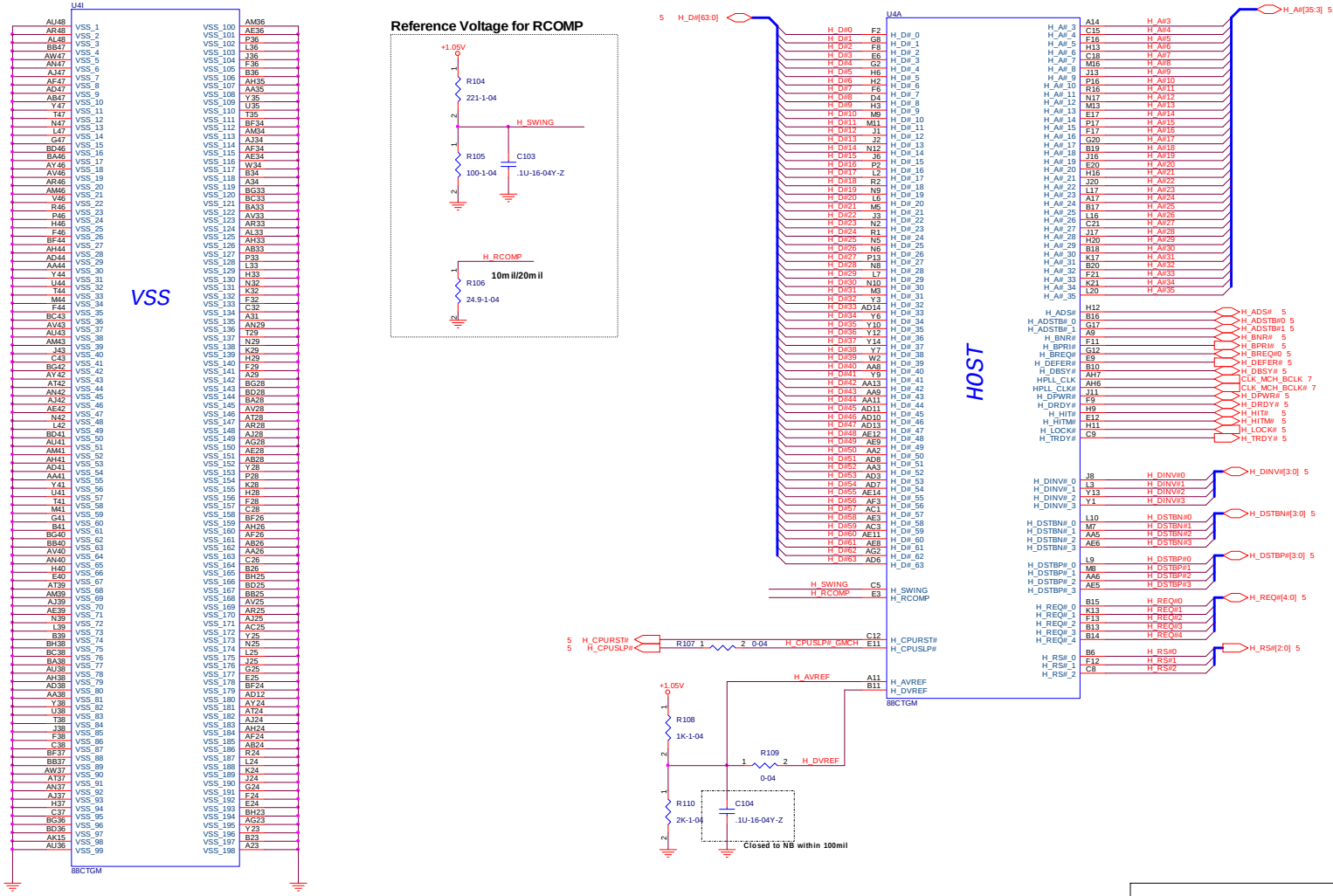

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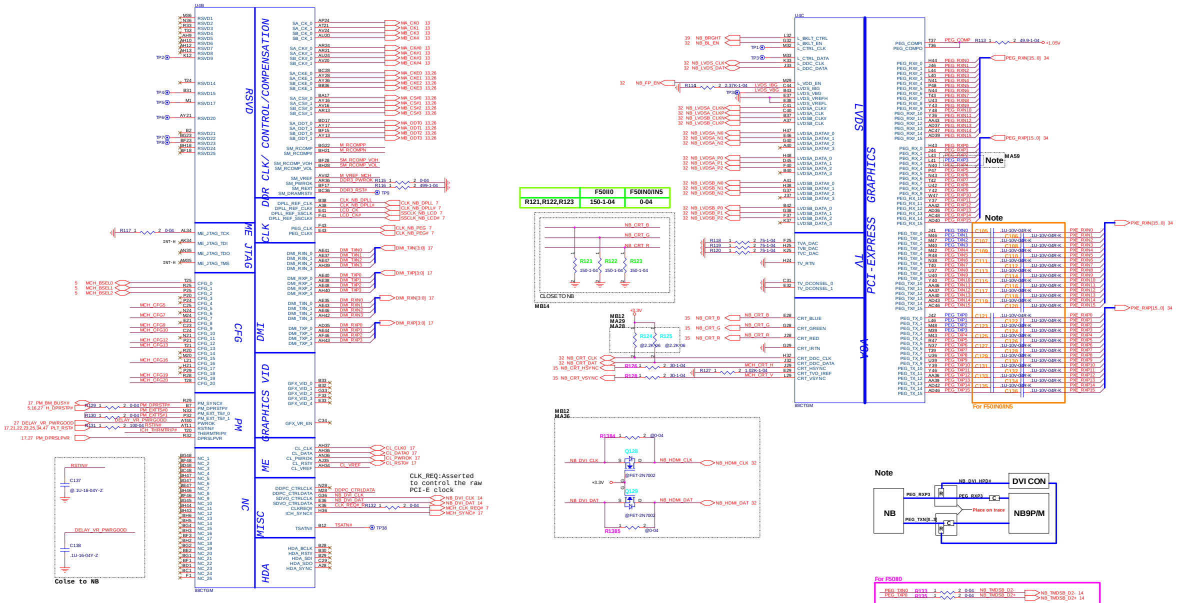
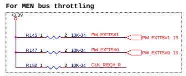


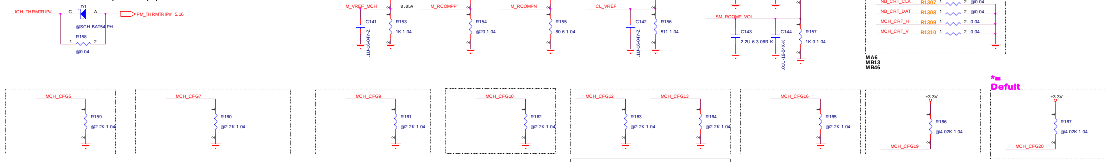
R121,R122,R123	F50II0	F50IN0/IN5
	150-1-04	0-04

For MEN bus throttling



MCH_BSEL2	MCH_BSEL1	MCH_BSEL0	FSB
0	0	0	1066
0	1	0	800
0	1	1	667

Reserve for NB THRMTRIP# (O/D Vccp)



Defult

DMI X2 Select

MCH_CFG5	0 = DMIx2	
	1 = DMIx4	*

ME TLS Confidentiality (Isolation Bypass Enable)

MCH_CFG7	0 = AMT Firmware will use TLS cipher suite with no confidentiality	
	1 = AMT Firmware will use TLS cipher suite with Confidentiality	*

PCI Express Graphics Lane

MCH_CFG9	0 = Reverse Lane	
	1 = Normal operation	*

PCIE Loopback enable

MCH_CFG10	0 = Enabled	
	1 = Disabled	*

XOR / ALLZ / Clock Un-gating

CFG12	CFG13	Configuration
0	0	Clock Gating Disabled
0	1	XOR Mode Enabled
1	0	All-Z Mode Enabled
1	1	Normal Operation *

FSB Dynamic ODT

MCH_CFG16	0 = Dynamic ODT Disabled	
	1 = Dynamic ODT Enabled	*

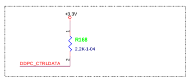
DMI Lane Reversal

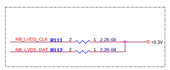
MCH_CFG19	0 = Normal	*
	1 = Lanes Reversed	

ME TLS Confidentiality (Isolation Bypass Enable)

MCH_CFG20	0 = Only SDVO or PCIE x1 is operational	*
	1 = SDVO and PCIE x1 are operating simultaneously via the PEG port	

MB45
MB13
MA36





MB44

SDVO_CTRLDATA (NB_DVI_DAT)		
F50IN0/IN5	0 = SDVO/HDMI/DP interface Disabled (PCIE Enable) *	R205 option
F50II0	1 = SDVO/HDMI/DP interface Enabled	R205 mount

*	NB_DVI_DAT	NB_DVI_CLK	FUNCTION
CH7318	2.2K pull up	2.2K pull up	
PS8101	47K pull up	47K pull up	DDCBUF_EN = LOW : DDC Passive Buffer (default)
	1.5K pull up	1.5K pull up	DDCBUF_EN = HIGH : DDC Active Buffer

DDPC_CTRLDATA		
F50IN0/IN5	0 = Digital display (HDMI/DP) device absent *	R168 option
F50II0	1 = Digital display (HDMI/DP) Device Present	R168 mount

L_DDC_DATA	0 = LFP Disabled	*
	1 = LFP Card Present; PCIE disabled	

UMA & HYBRID HW SRAP

STRAP	MCH_CFG9	SDVO_CTRLDATA	MCH_CFG20	DDPC_CTRLDATA	L_DDC_DATA
UMA	1	1	0	1	1
HYBRID (Entry/Middle range)	1	0	0	0	1

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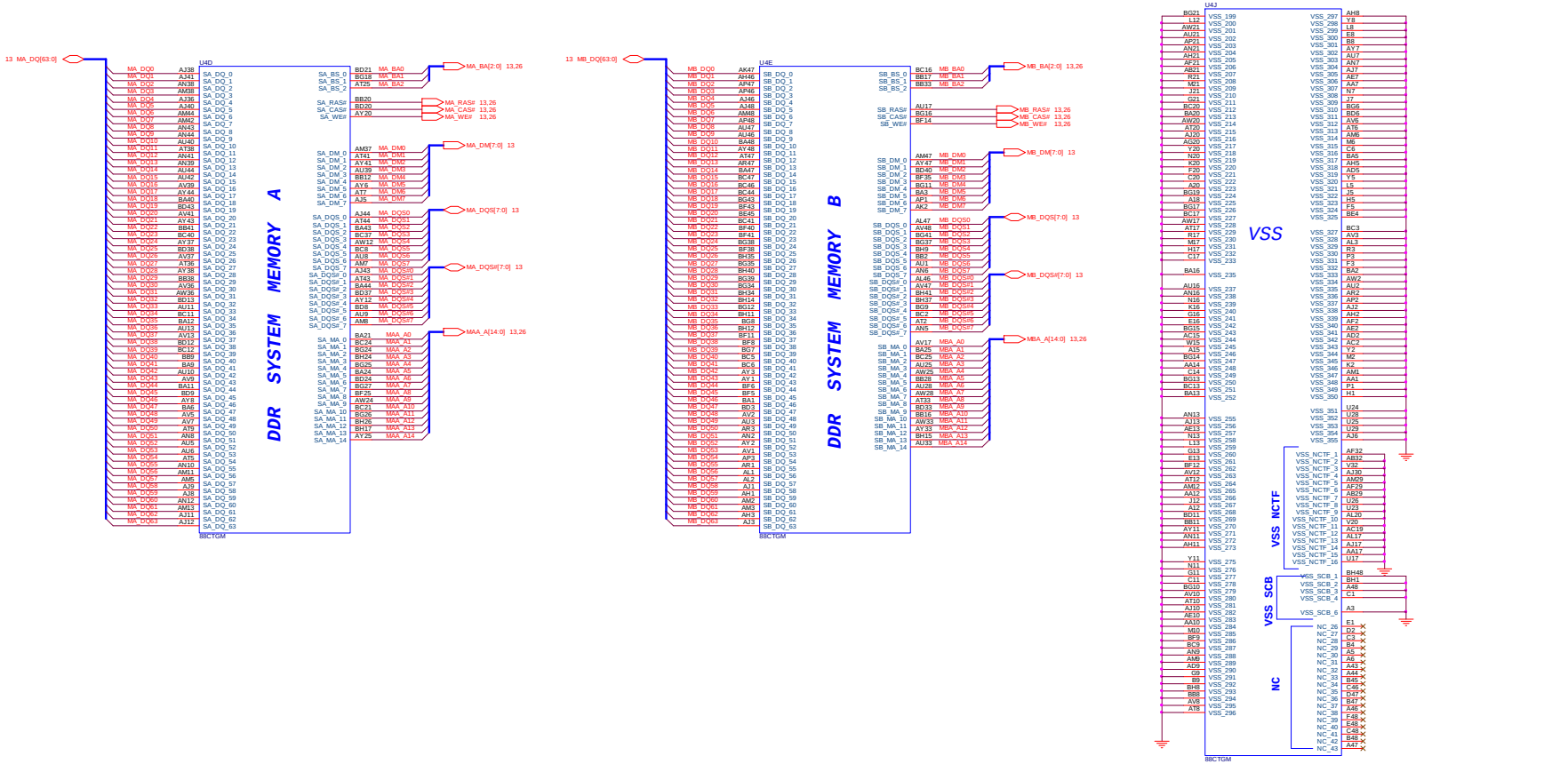

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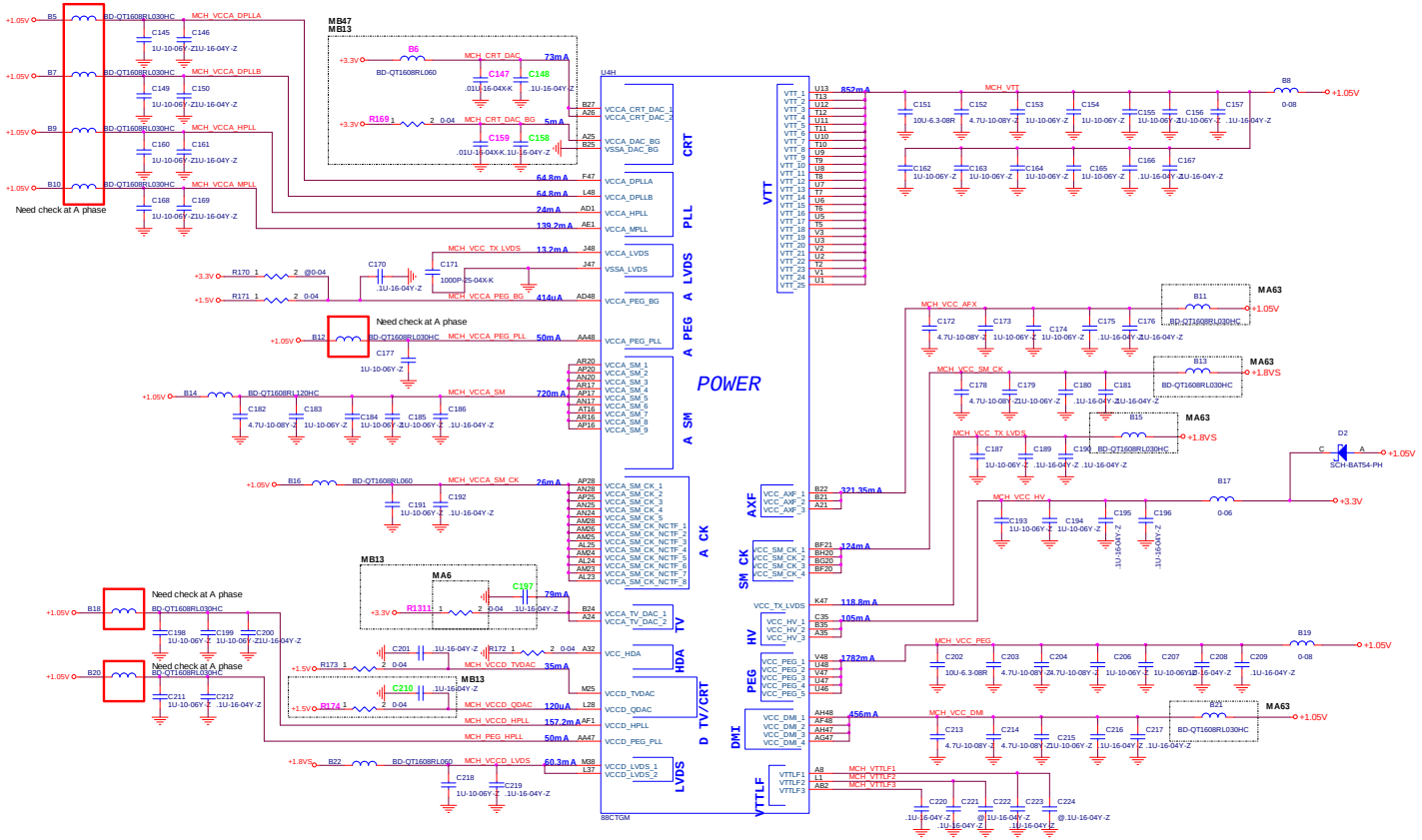
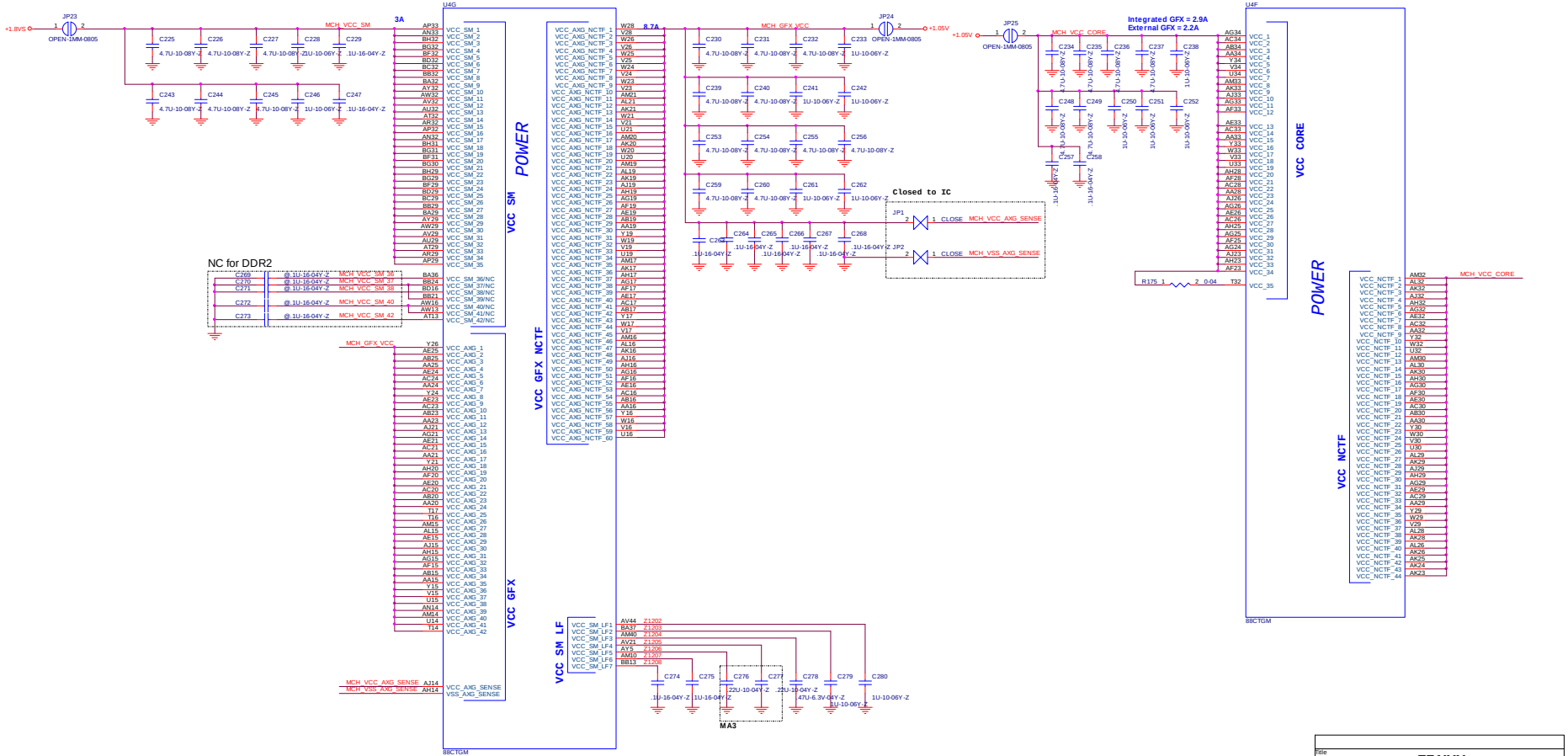
	F50II0	F50IN0/IN5
C148,C158,C197,C210	.1U-16-04Y-Z	0-04





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Size: Custom	Document Number: F71IXX	NB GFX/VCC/NCTF POWER	Rev: C
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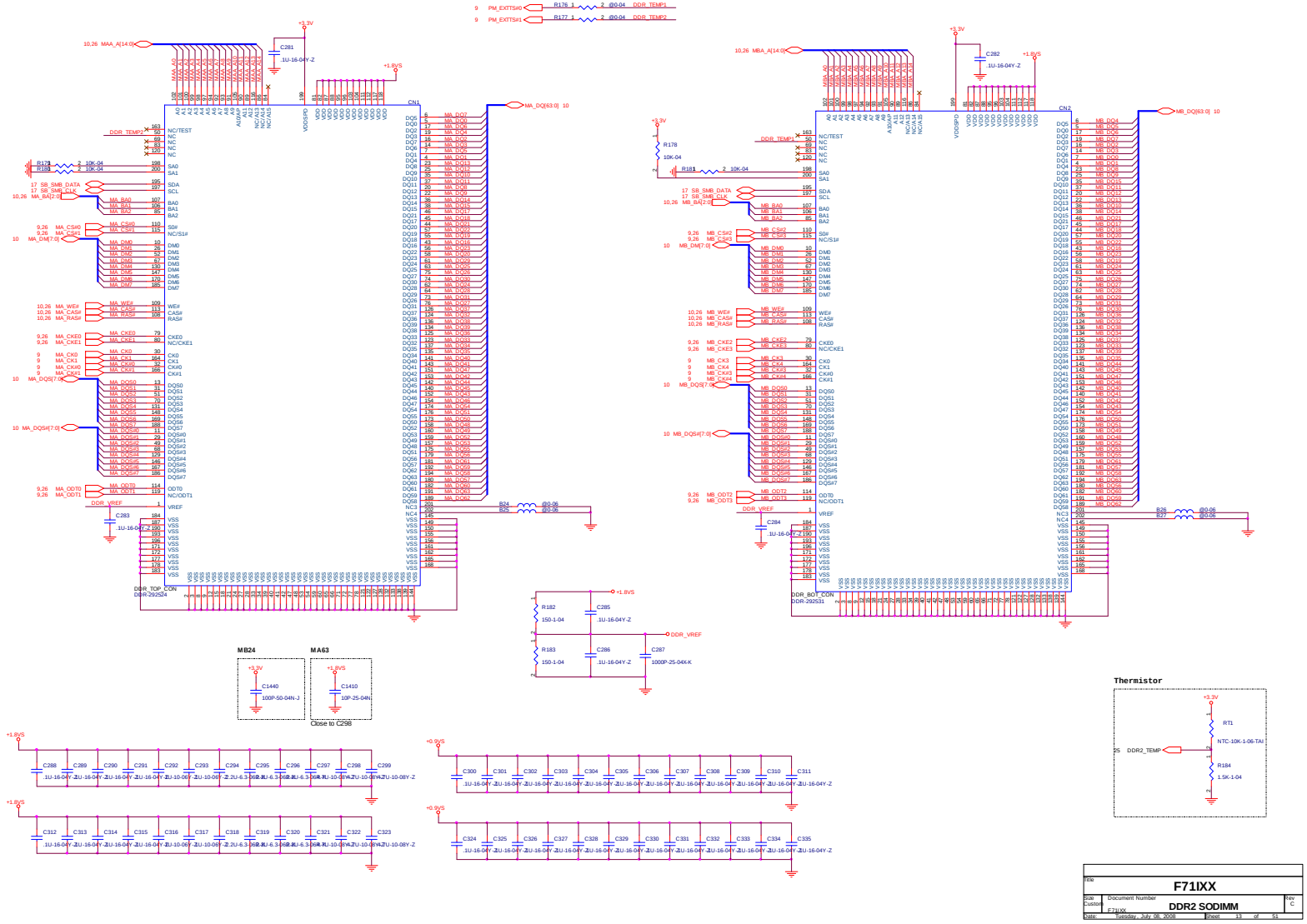
CN1
CN2
DDR_TOP_CON
DDR-292524
DDR_BOT_CON
DDR-292531
MB24
MA63
Close to C298
Thermistor
RT1
NTC-10K-1-06-TAI
R184
1.5K-1.04
DDR2_TEMP
F71IXX
DDR2 SODIMM
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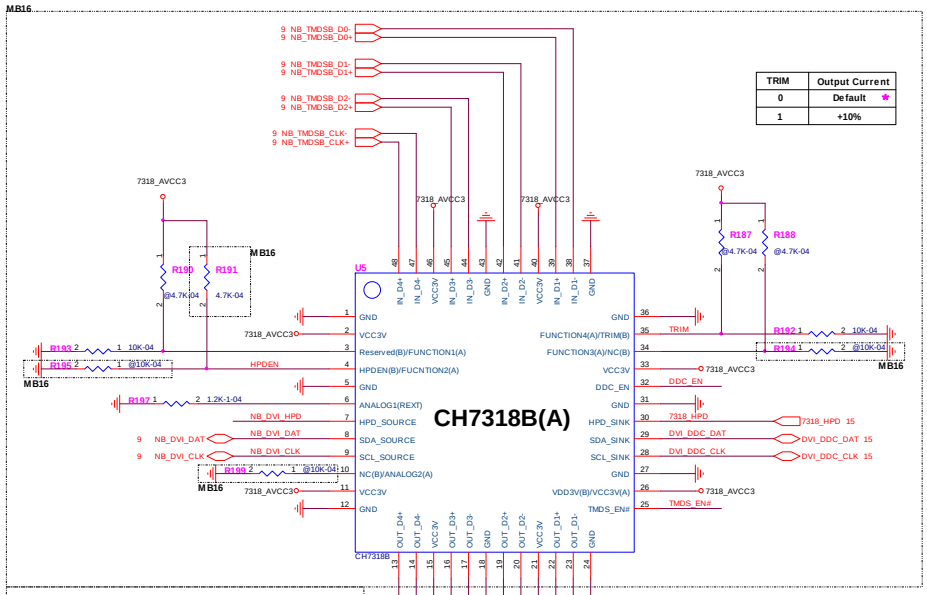
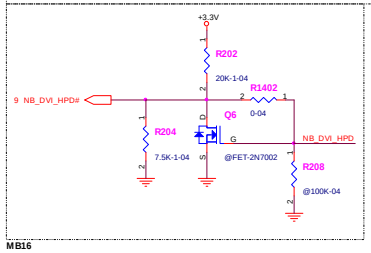
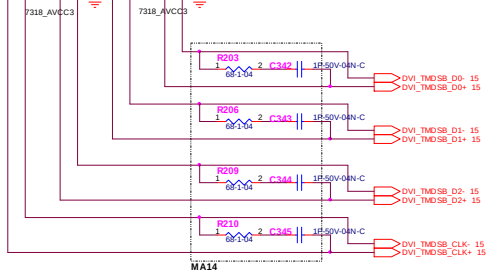


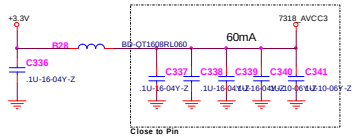
TRIM	Output Current
0	Default *
1	+10%

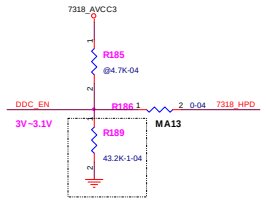


Location	CH7318A	CH7318B *
Q6	Mount	Option
R208	Mount	Option
R1402	Option	Mount

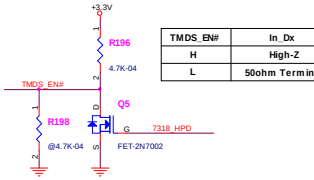
HPDEN	HPD_SOURCE
0	Non-inverting output
1	Inverting output(Open drain) *







DDC EN	Passgate
L	Disable
H	Enable



TMDS_EN#	In_Dx	TMDS_OUTx
H	High-Z	High-Z
L	50ohm Termination	Level shifting mode enabled

	NB_DVI_DAT	NB_DVI_CLK	FUNCTION
CH7318 *	2.2K pull up	2.2K pull up	
PS8101	47K pull up	47K pull up	DDCBUF_EN = LOW : DDC Passive Buffer (default)
	1.5K pull up	1.5K pull up	DDCBUF_EN = HIGH : DDC Active Buffer

Pin	CH7318B *	PS8101
3	10K pull down	4.7K pull up
4	4.7K pull up	
6	1.2K_1	499R_1
10	NC	
28	2.2K pull up	1.5K pull up
29	2.2K pull up	1.5K pull up
32	20K pull down	4.7K pull up
34	NC	4.7K pull up
35	10K pull down	4.7K pull up
13,14	Mount R210,C345	Option R210,C345
16,17	Mount R209,C344	Option R209,C344
19,20	Mount R206,C343	Option R206,C343
22,23	Mount R203,C342	Option R203,C342

Title: **F71IXX**

Size: Custom | Document Number: F71IXX | **NB DVI LEVEL SHIFT** | Rev: C

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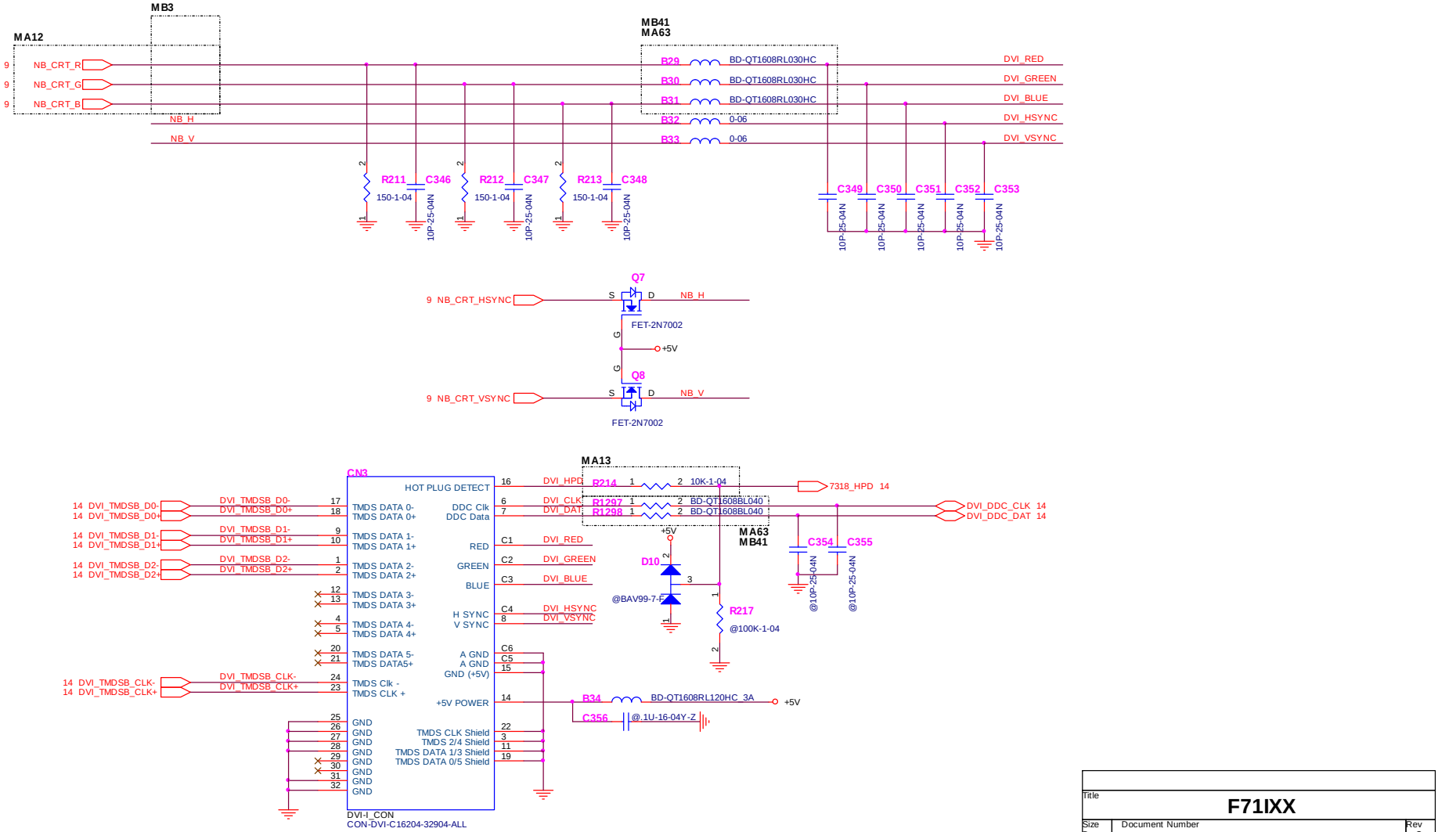

Title	F71IXX		
Size B	Document Number F71IXX	NB DVI-I CON	Rev C
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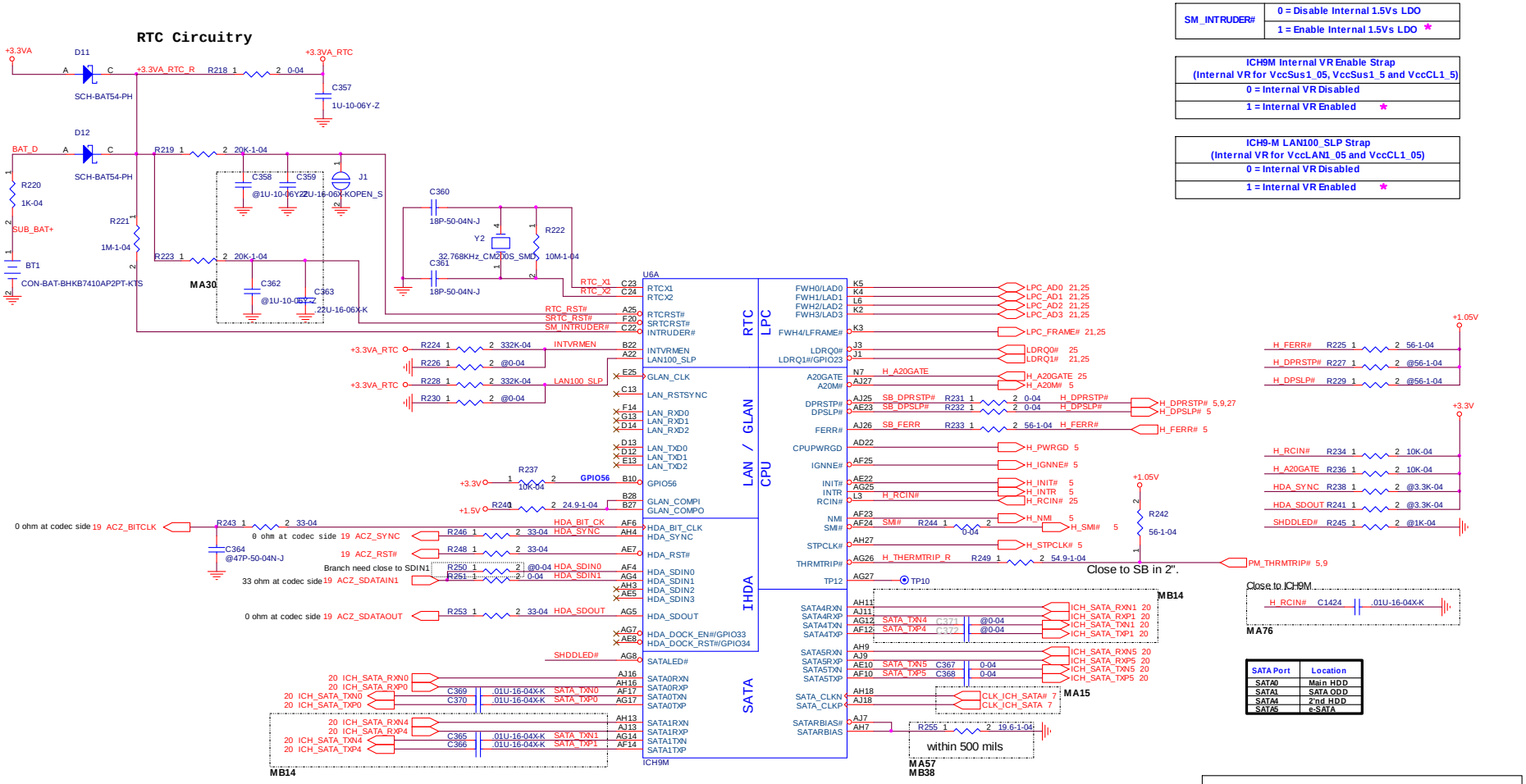
RTC Circuitry
SM_INTRUDER#
0 = Disable Internal 1.5Vs LDO
1 = Enable Internal 1.5Vs LDO *
ICH9M Internal VR Enable Strap
(Internal VR for VccSus1_05, VccSus1_5 and VccCL1_5)
0 = Internal VR Disabled
1 = Internal VR Enabled *
ICH9-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1_05)
0 = Internal VR Disabled
1 = Internal VR Enabled *
SATA Port
Location
SATA0
Main HDD
SATA1
SATA ODD
SATA4
2'nd HDD
SATA5
e-SATA
Close to SB in 2".
Close to ICH9M
within 500 mils
Title
F71IXX
Size
Custom
Document Number
F71IXX
ICH9M RTC/SATA/HDA/LPC 1/3
Rev
C
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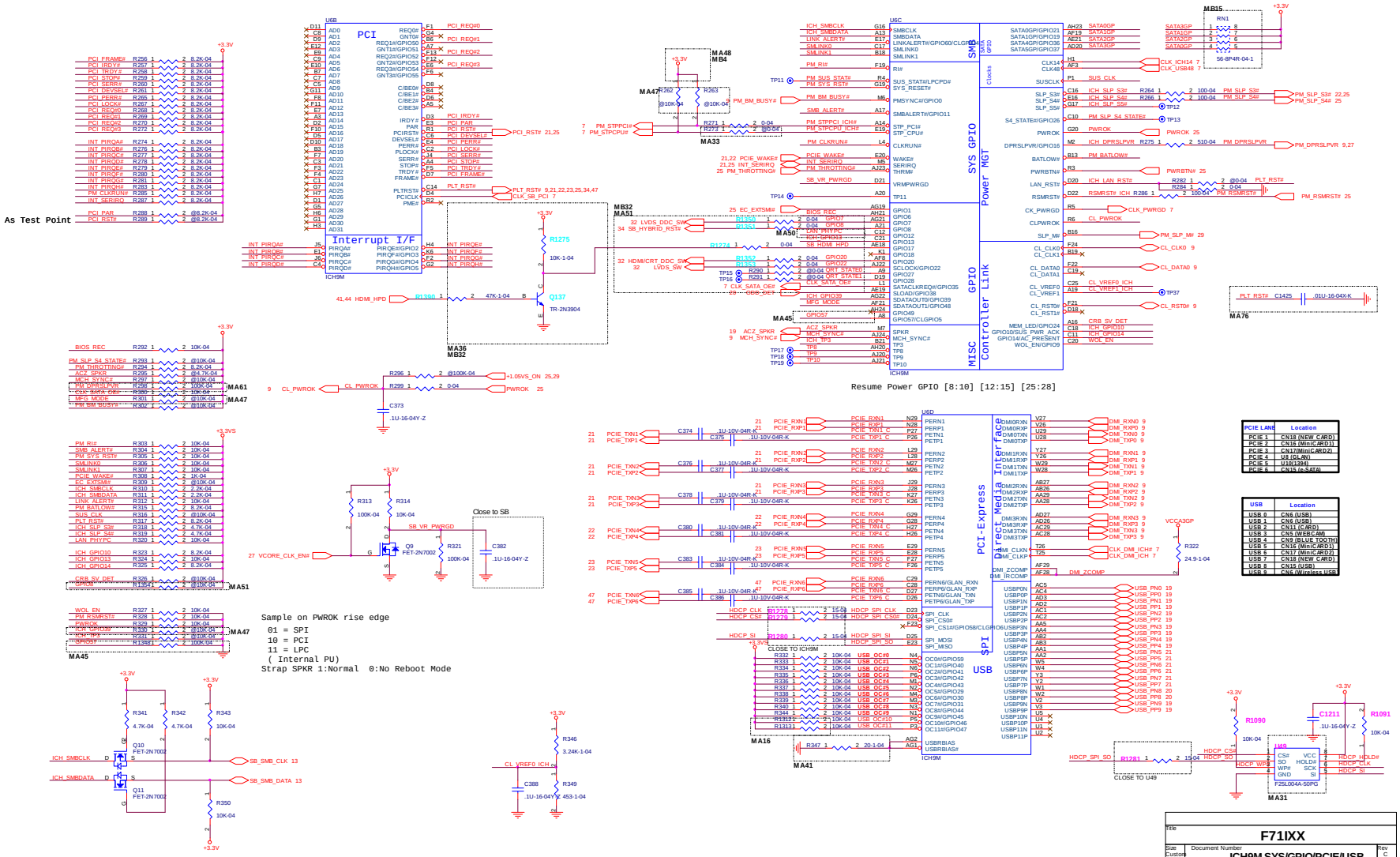
51


As Test Point
PCI
Interrupt I/F
ICH9M
Resume Power GPIO [8:10] [12:15] [25:28]
Sample on PWROK rise edge
01 = SPI
10 = PCI
11 = LPC
(Internal PU)
Strap SPKR 1:Normal 0:No Reboot Mode
Close to SB
CLOSE TO ICH9M
CLOSE TO U49
PCIE LANE | Location
PCIE 1 | CN18 (NEW CARD)
PCIE 2 | CN16 (MiniCARD1)
PCIE 3 | CN17(MiniCARD2)
PCIE 4 | U8 (GLAN)
PCIE 5 | U30(1394)
PCIE 6 | CN15 (e-SATA)
USB | Location
USB 0 | CN6 (USB)
USB 1 | CN6 (USB)
USB 2 | CN11 (CARD)
USB 3 | CN5 (WEBCAM)
USB 4 | CN9 (BLUE TOOTH)
USB 5 | CN16 (MiniCARD1)
USB 6 | CN17 (MiniCARD2)
USB 7 | CN18 (NEW CARD)
USB 8 | CN15 (USB)
USB 9 | CN6 (Wireless USB
F71IXX
ICH9M SYS/GPIO/PCIE/USB
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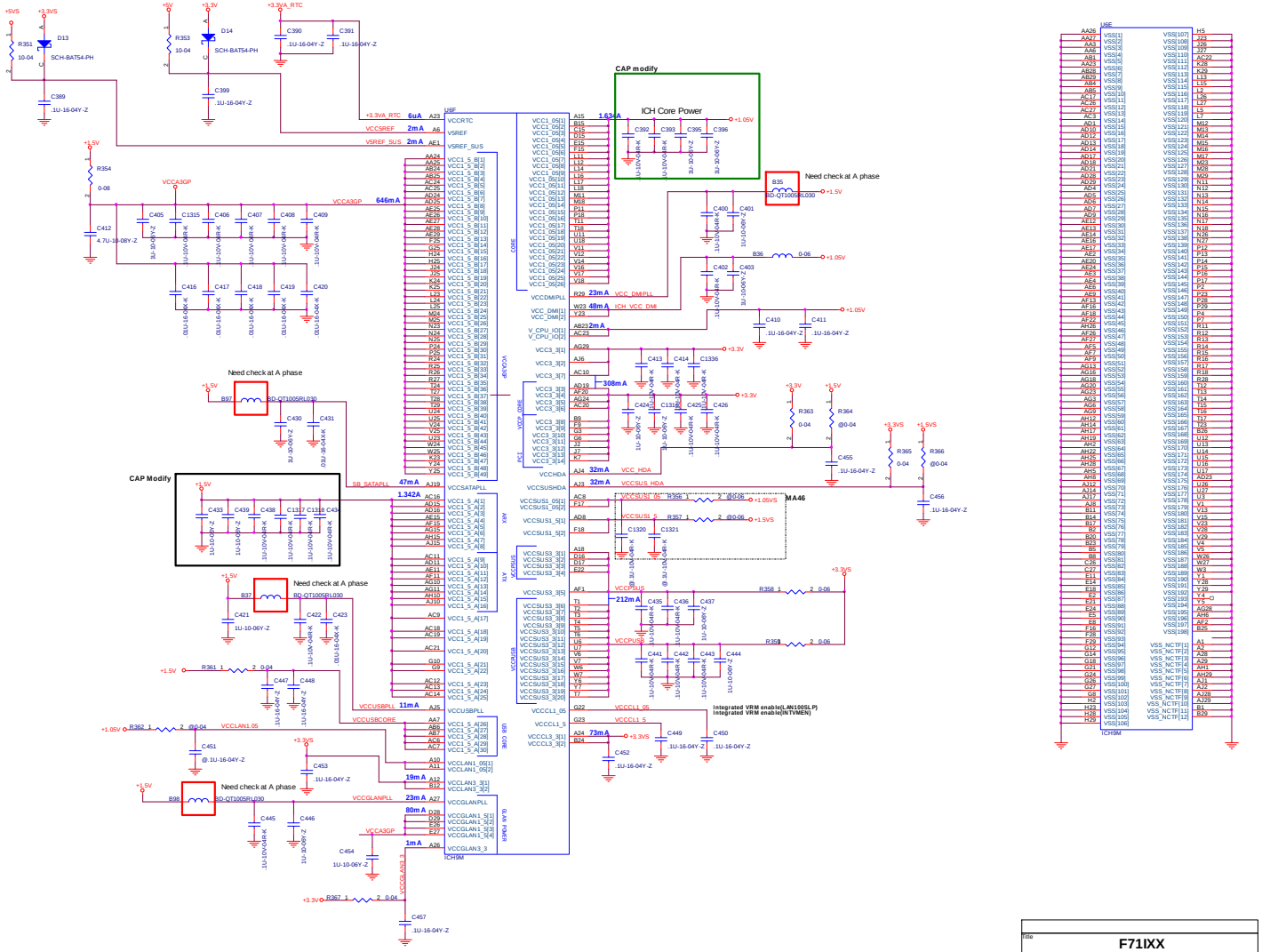

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Size: Custom	Document Number: F71IXX	Rev: C
	ICH9M Power	
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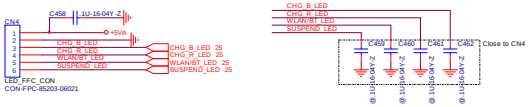
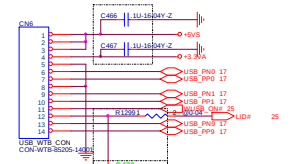
LED CON



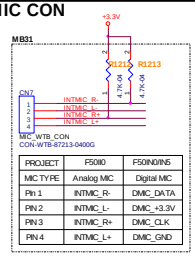
USB CON



C470	
LID#	.1U-16-04Y-Z
N/A	0-04

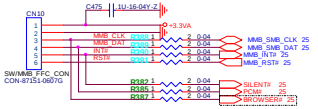
WUSB/BT_ON#	
0	ON
1	OFF

D/A MIC CON

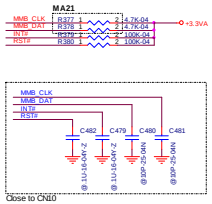


PROJECT	F50I0	F50IND/IN5
MIC TYPE	Analog MIC	Digital MIC
Pin 1	INTMIC_R-	DMIC_DATA
PIN 2	INTMIC_L-	DMIC_+3.3V
PIN 3	INTMIC_R+	DMIC_CLK
PIN 4	INTMIC_L+	DMIC_GND

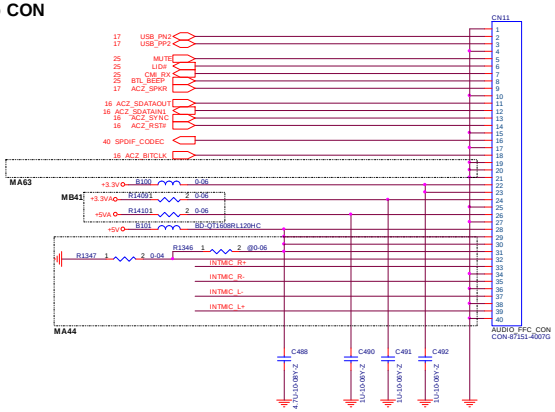
SW / MMB CON



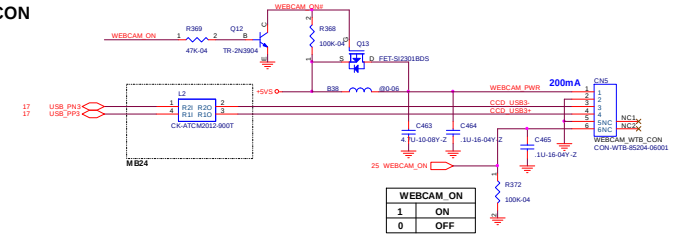
Resirtor Option	
F50II0/IIN0	R382,R385,R387
F50IN5	R388,R389,R390,R391



Audio CON

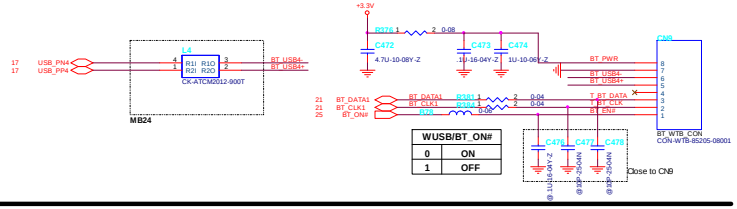


WEBCAM CON



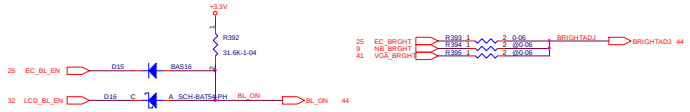
WEBCAM_ON	
1	ON
0	OFF

BLUETOOTH CON

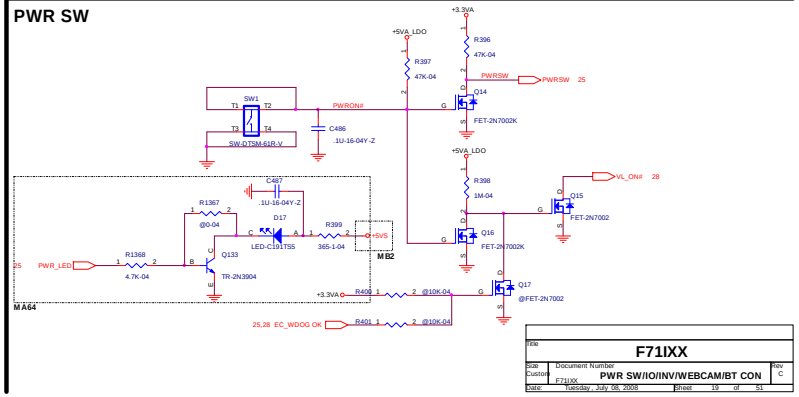


WUSB/BT_ON#	
0	ON
1	OFF

INVERTER



PWR SW



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Size: Custom	Document Number: F71IXX	PWR SW/IO/INV/WEBCAM/BT CON	Rev: C
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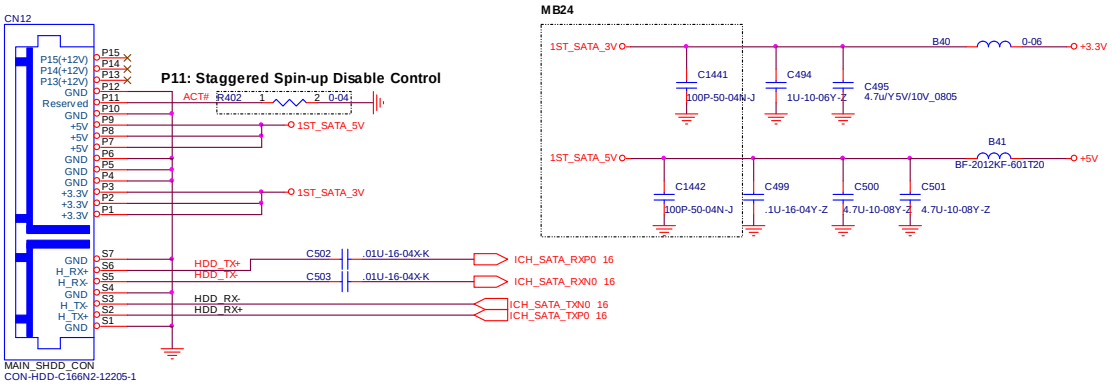
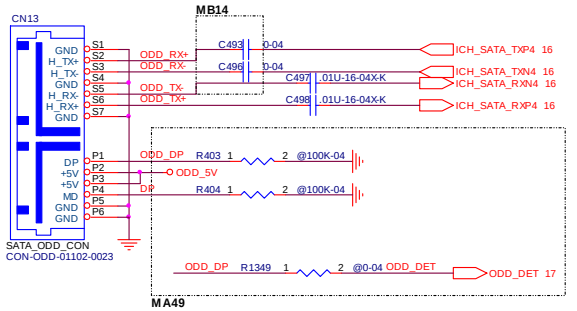
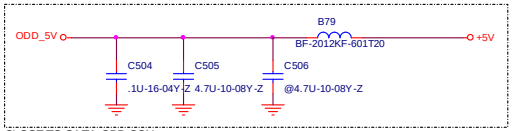
MASTER HDD CON



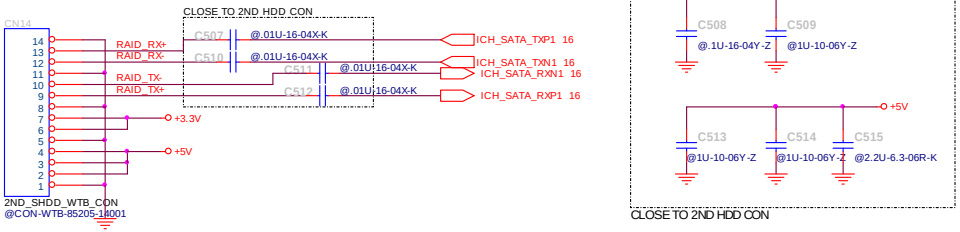
SATA ODD CON

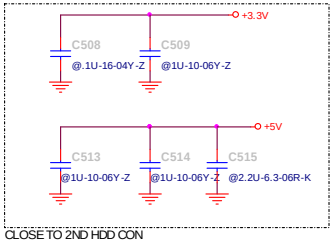




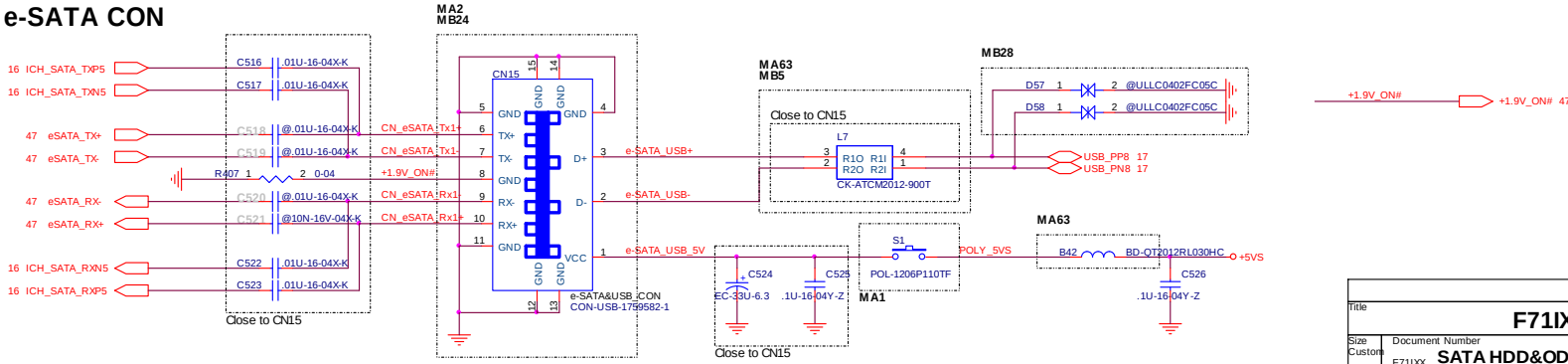
2ND HDD CON

RESERVED FOR 17" 2ND HDD





e-SATA CON



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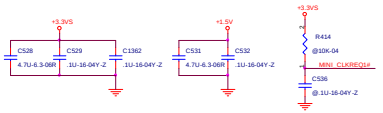
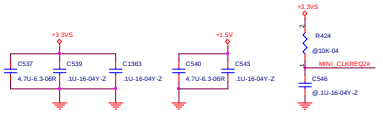
MINI CARD CON

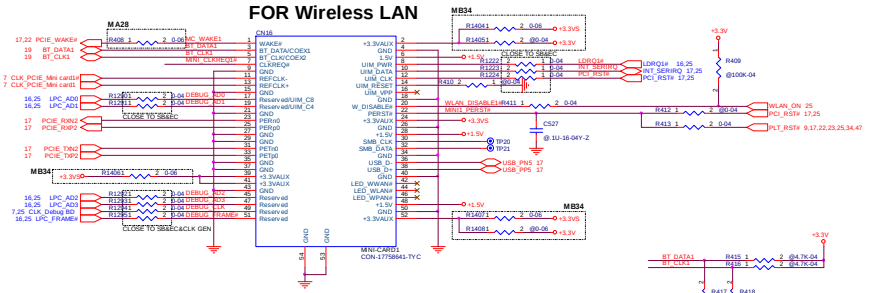
Intel PRO/Wireless 2100 LAN

PIN11	LED_WLAN_LINK	H(3.3V)	Solid ON	Associated AP
			1 flash/3 sec	Not Associated with an AP
		Low(0V)	LED OFF	Power OFF or RF_Kill active
PIN12	LED_WLAN_ACT	H(3.3V)	Rapid Blinking	Passing data traffic to AP
			Slow Blinking	Beacon traffic to Ap
		Low(0V)	LED OFF	Power OFF or not activity or RF_Kill active
PIN13	HW_RadioXMT_OFF#	H(3.3V)	Enable	Radio transmitter is ON
		Low(0V)	Disable	Radio transmitter turn off

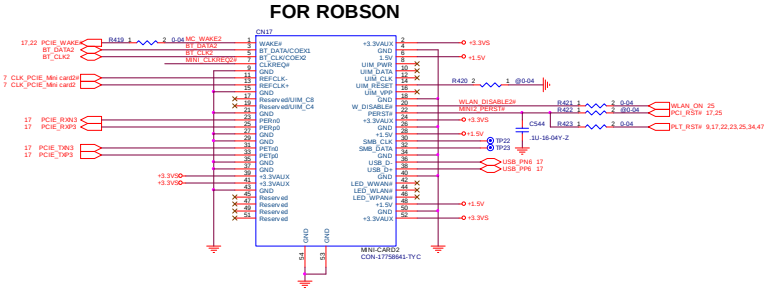




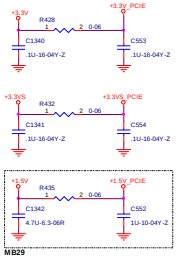
FOR Wireless LAN

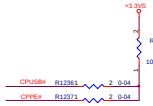


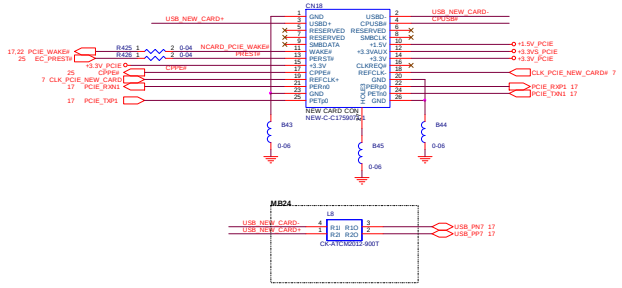
FOR ROBSON



NEW CARD SOCKET







Title	F71IXX		
Size: Custom	Document Number: F71IXX	Mini Card / New Card CON	Rev: C
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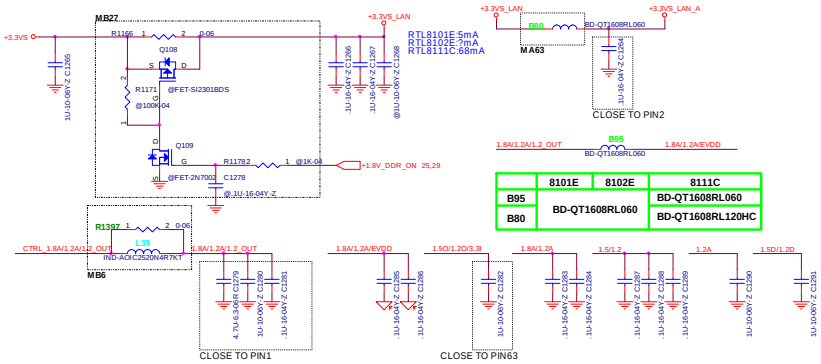
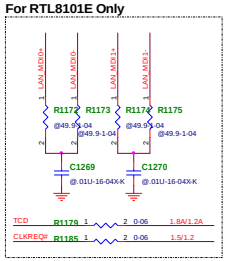
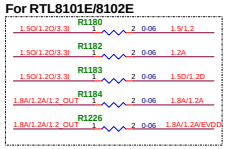
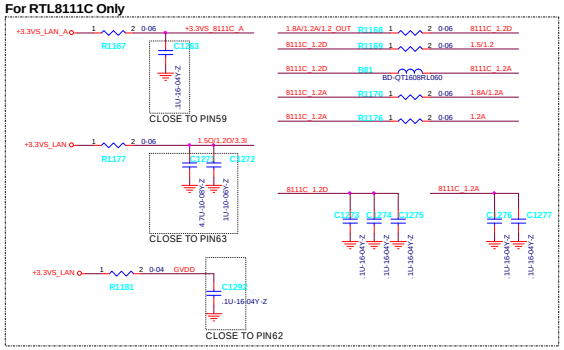


	8101E	8102E	8111C
B95	BD-QT1608RL060		BD-QT1608RL060
B80			BD-QT1608RL120HC

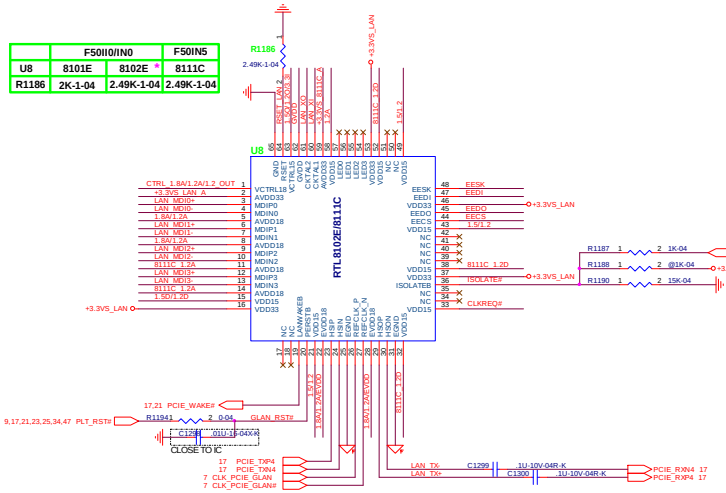


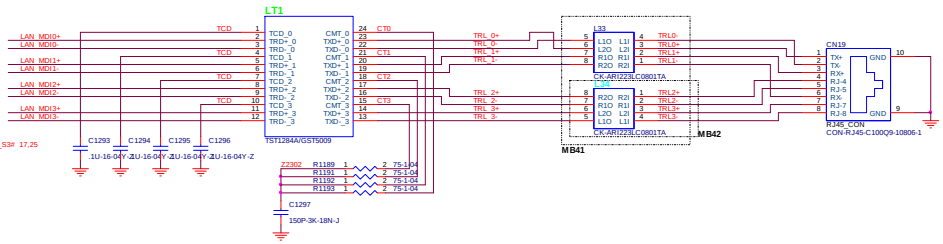




Project	F50II0/IN0 (10/100 LAN)	F50IN5 (Giga LAN)
LT1	XMER-TST1284A	XMER-GST5009

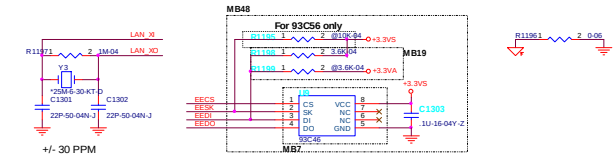
	F50II0/IN0		F50IN5
U8	8101E	8102E *	8111C
R1186	2K-1-04	2.49K-1-04	2.49K-1-04





Power Consumption Chart

	RTL8101E		RTL8102E		RTL8111C	
+3.3VS_LAN	*3.3V*	5mA	*3.3V*	?mA	*3.3V*	68mA
1.8A/1.2A	*1.8V*	175mA	*1.2V*	?mA	*1.2V*	331mA
1.5/1.2	*1.5V*	72mA	*1.2V*	?mA	*1.2V*	



Title	F71IXX		
Size: Custom	Document Number: F71IXX	LAN RTL8102E / RTL8111C	Rev: C
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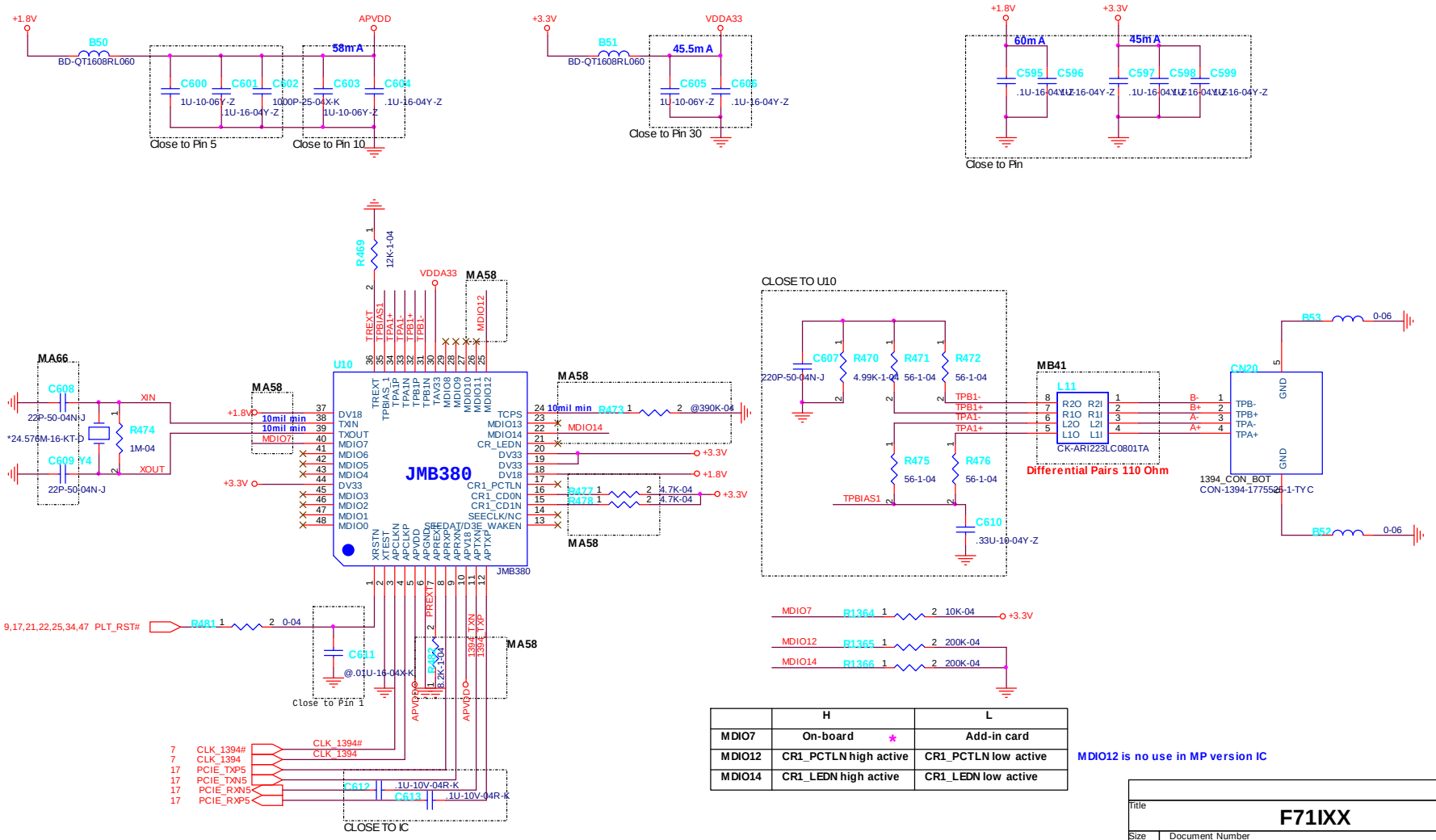

	H	L
MDIO7	On-board *	Add-in card
MDIO12	CR1_PCTLN high active	CR1_PCTLN low active
MDIO14	CR1_LEDN high active	CR1_LEDN low active

MDIO12 is no use in MP version IC

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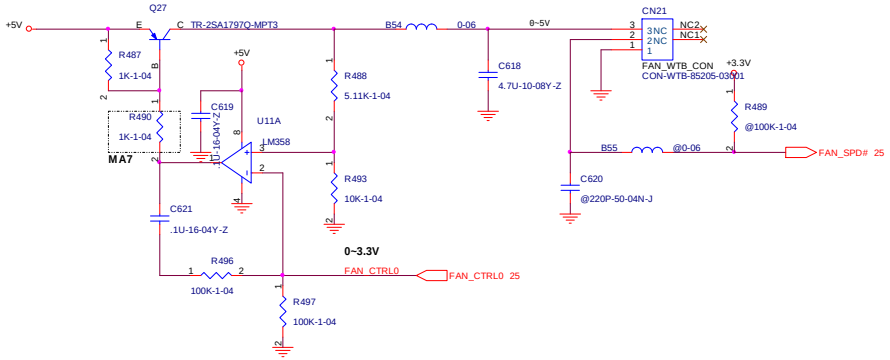
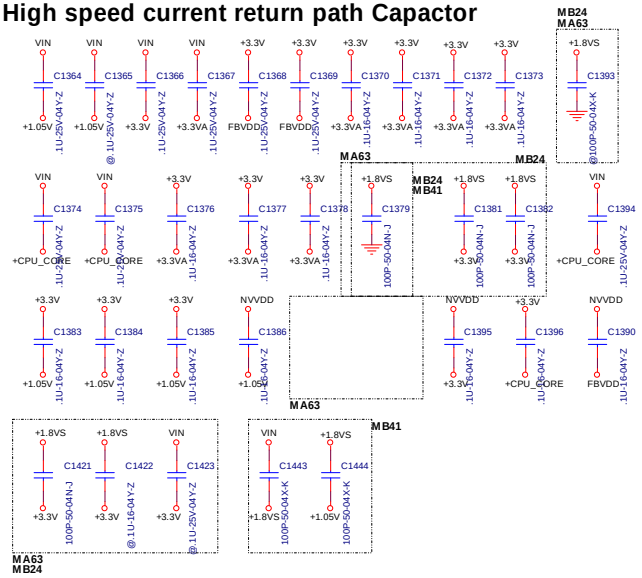
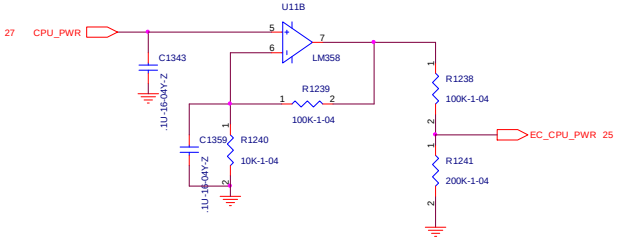
CPU FAN CONTROL



High speed current return path Capactor



CPU POWER MONITOR



Title	F71IXX		
Size: Custom	Document Number: F71IXX	CPU FAN/HSCRP CAP/V CORE SENS	Rev: C
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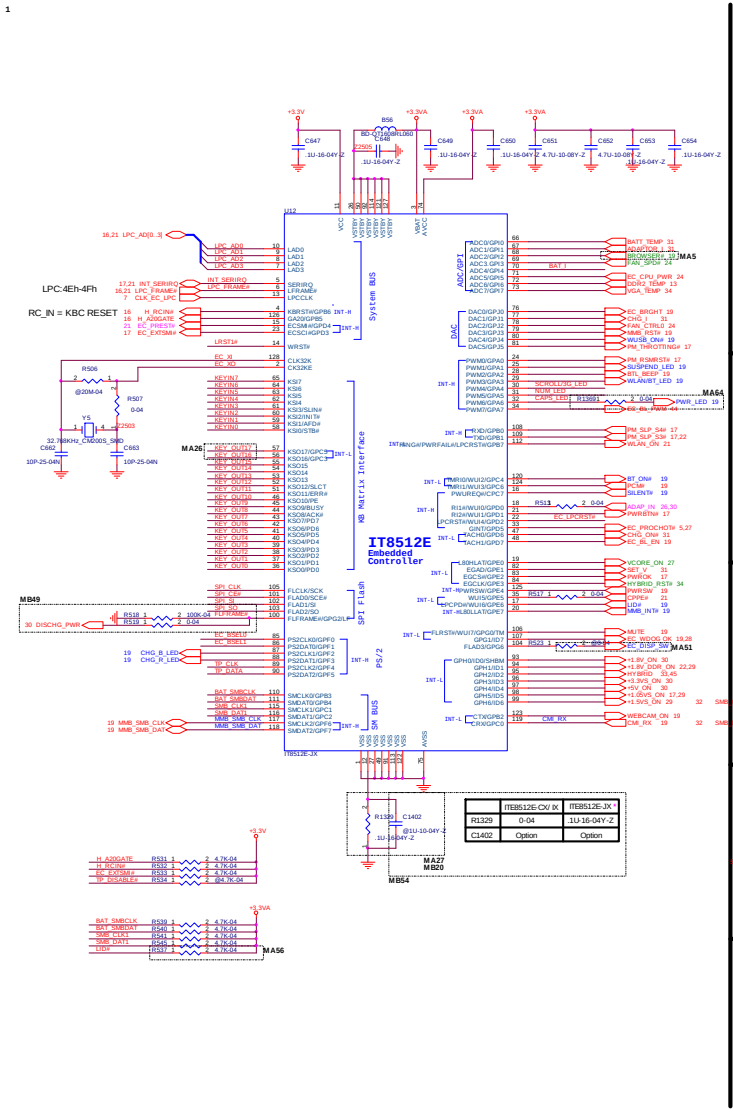
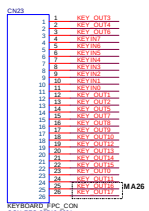
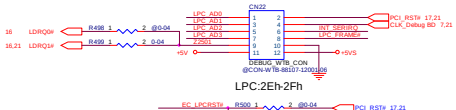


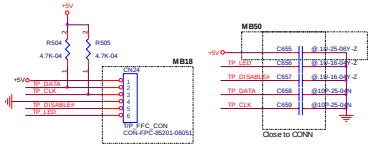
KEYBOARD CON



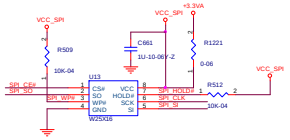
Debug BD CON



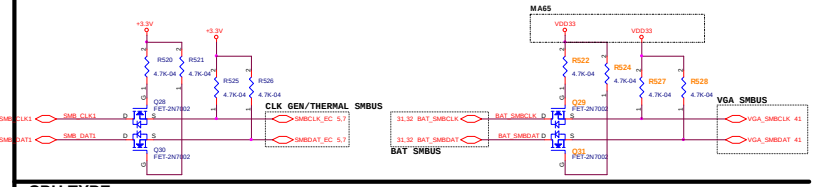
TP CON



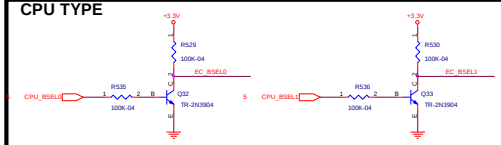
FLASH ROM(SPI)



SMBUS LEVEL SHIFT

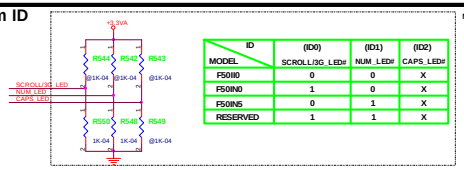


CPU TYPE



FSB \ BSEL	EC_BSEL2	EC_BSEL1	EC_BSEL0	MHZ
FSB667	X	0	0	166
FSB800	X	0	1	200
FSB1066	X	1	1	266

Platform ID



ID / MODEL	(ID0) SCROLL/3G_LED#	(ID1) NUM_LED#	(ID2) CAPS_LED#
F50II0	0	0	X
F50IN0	1	0	X
F50IN5	0	1	X
RESERVED	1	1	X

MA72

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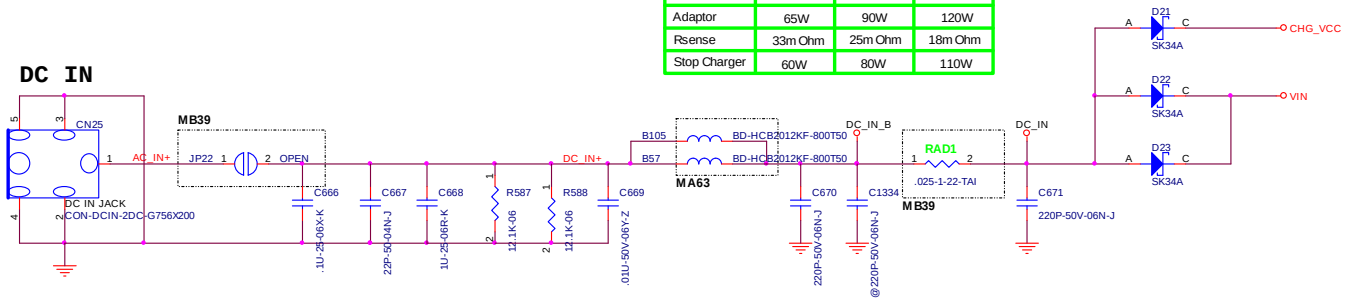
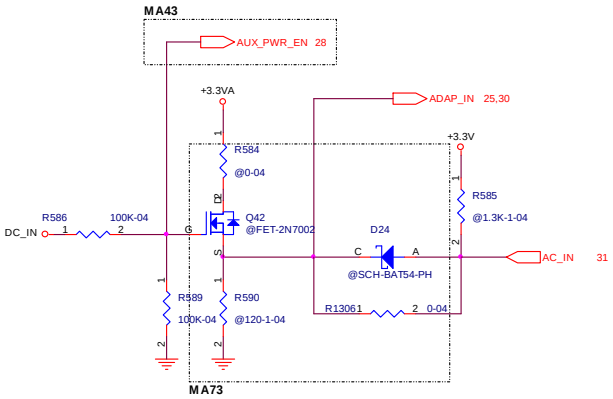
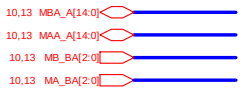
PROJECT	F50II0	F50IN0	F50IN5
Adaptor	65W	90W	120W
Rsense	33m Ohm	25m Ohm	18m Ohm
Stop Charger	60W	80W	110W

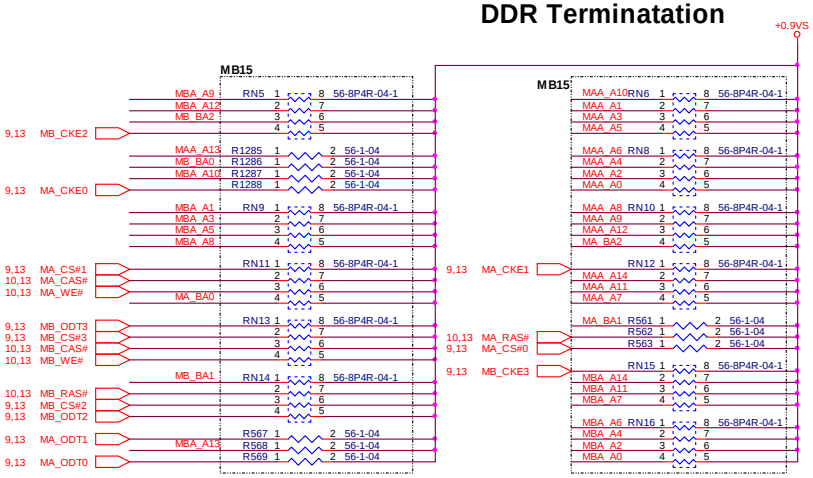
DC IN







DDR Terminatation



Title	F71IXX		
Size: Custom	Document Number: F71IXX	DC IN / SYS MEM TERMINATION	Rev: C
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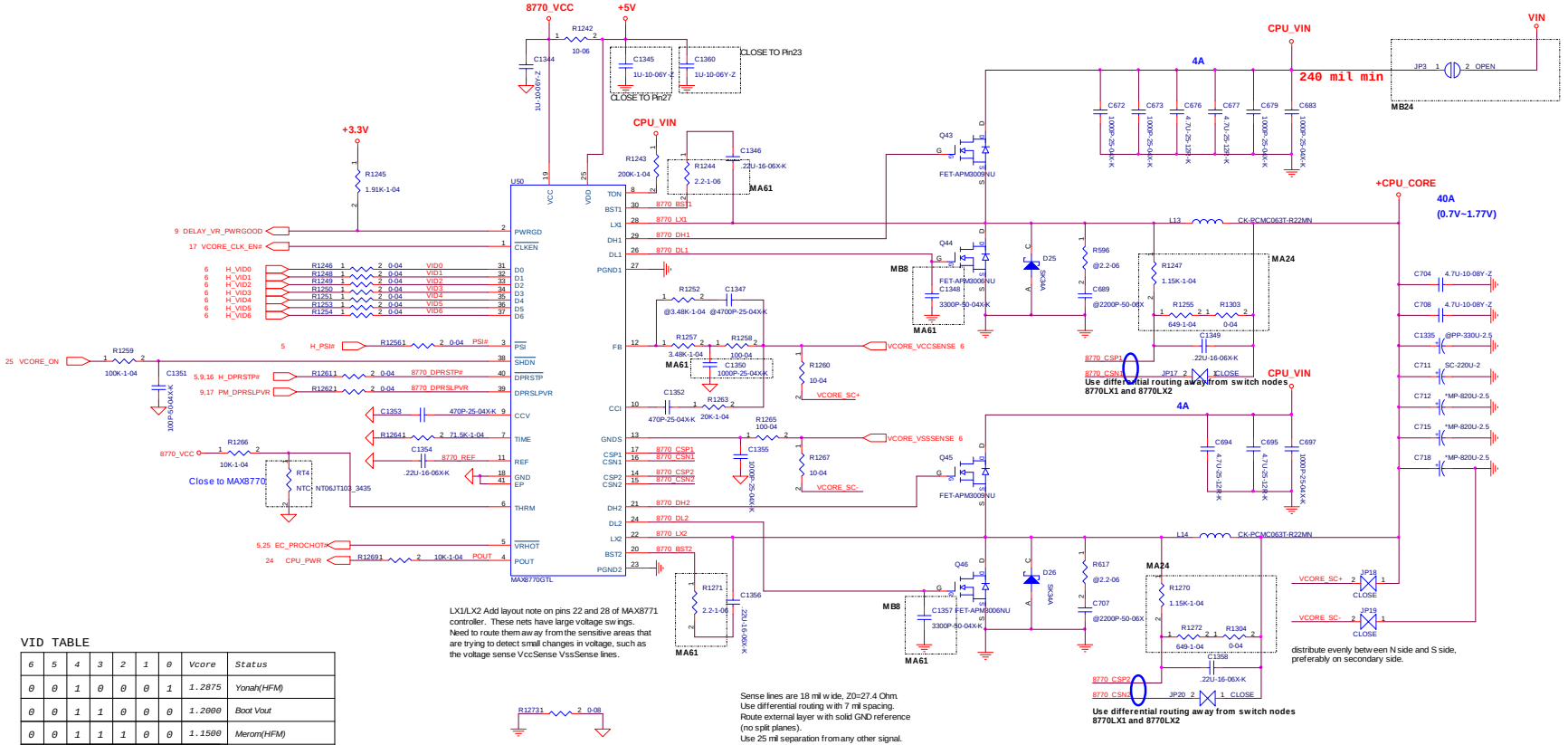

VID TABLE

6	5	4	3	2	1	0	Vcore	Status
0	0	1	0	0	0	1	1.2875	Yonah(HFM)
0	0	1	1	0	0	0	1.2000	Boot Vout
0	0	1	1	1	0	0	1.1500	Merom(HFM)
0	1	1	0	1	0	1	0.8375	Y&M(LFM)
0	1	1	1	0	1	1	0.7625	Y&M(Deeper Sleep)
1	1	1	1	1	1	1	0.0000	Shut down

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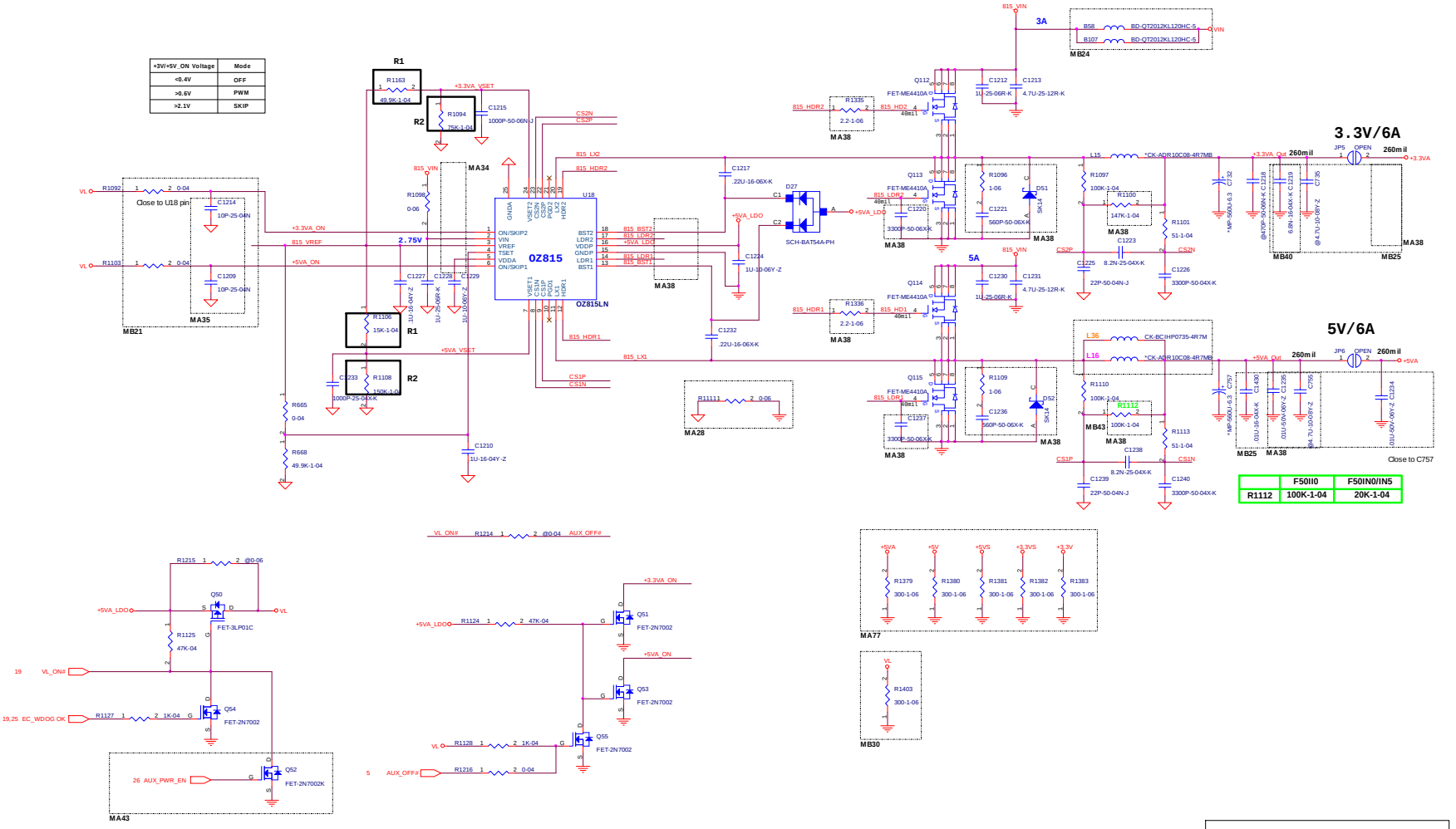
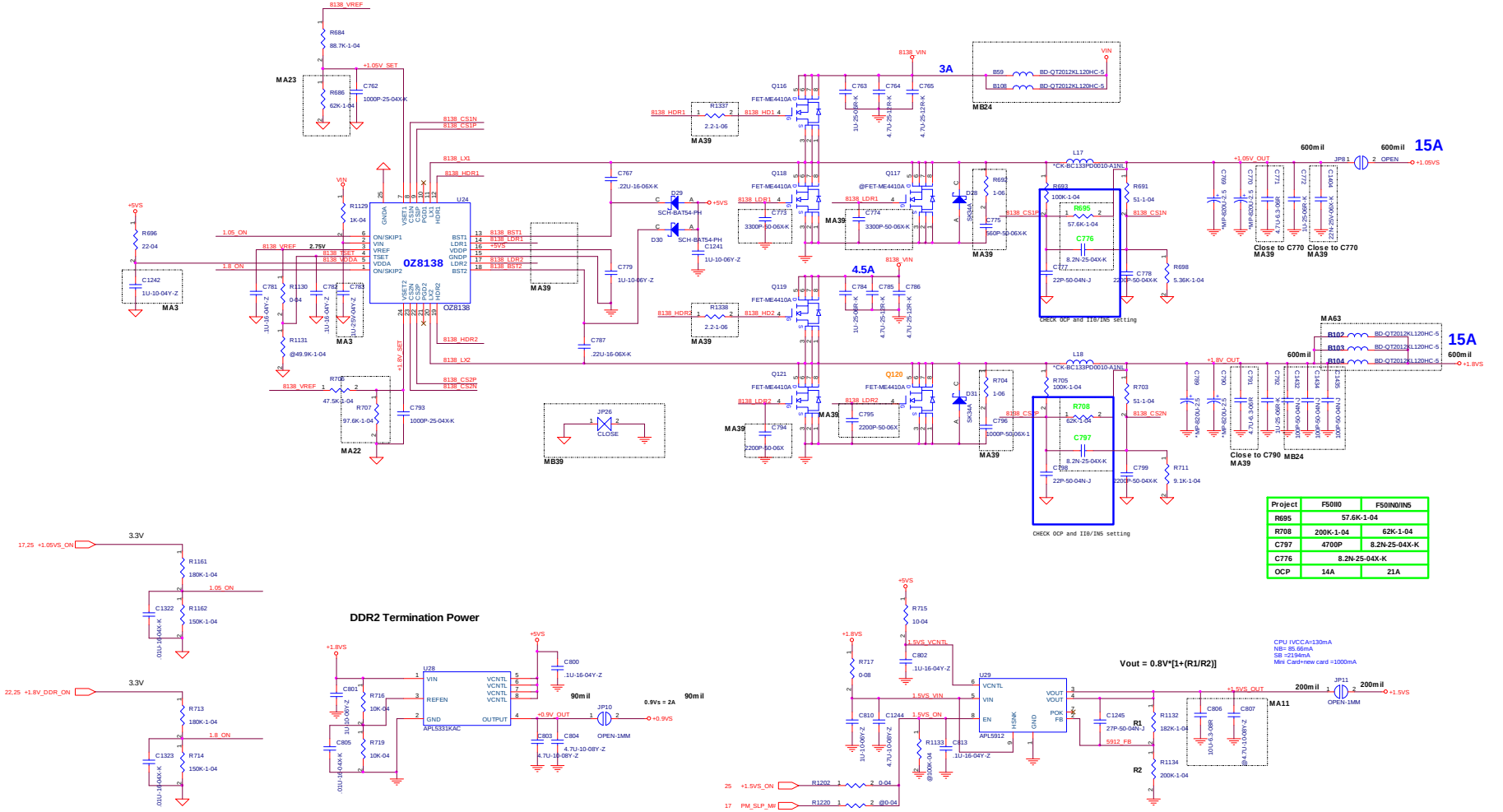
Output Voltage =[Vref x R2/(R1+R2)] x 2





Project	F50II0	F50IN0/IN5
R695	57.6K-1-04	
R708	200K-1-04	62K-1-04
C797	4700P	8.2N-25-04X-K
C776	8.2N-25-04X-K	
OCP	14A	21A

Title	F71IXX
Size: Custom	Document Number: F71IXX — 1.5VS/1.05VS/1.8VS — Rev: C
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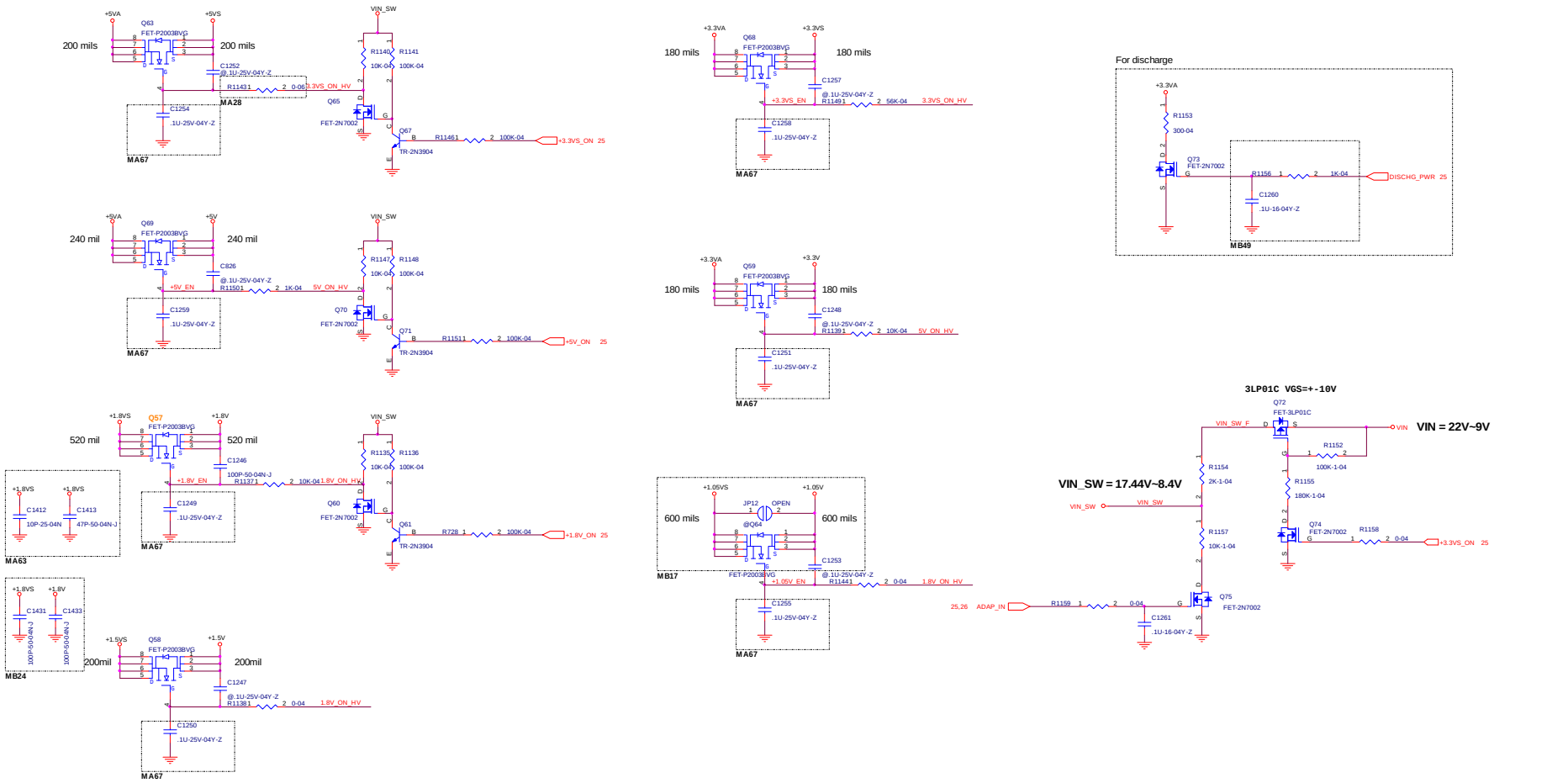

Title	F71IXX		
Size: Custom	Document Number: F71IXX	VCC SW/ VIN_SW	Rev: C
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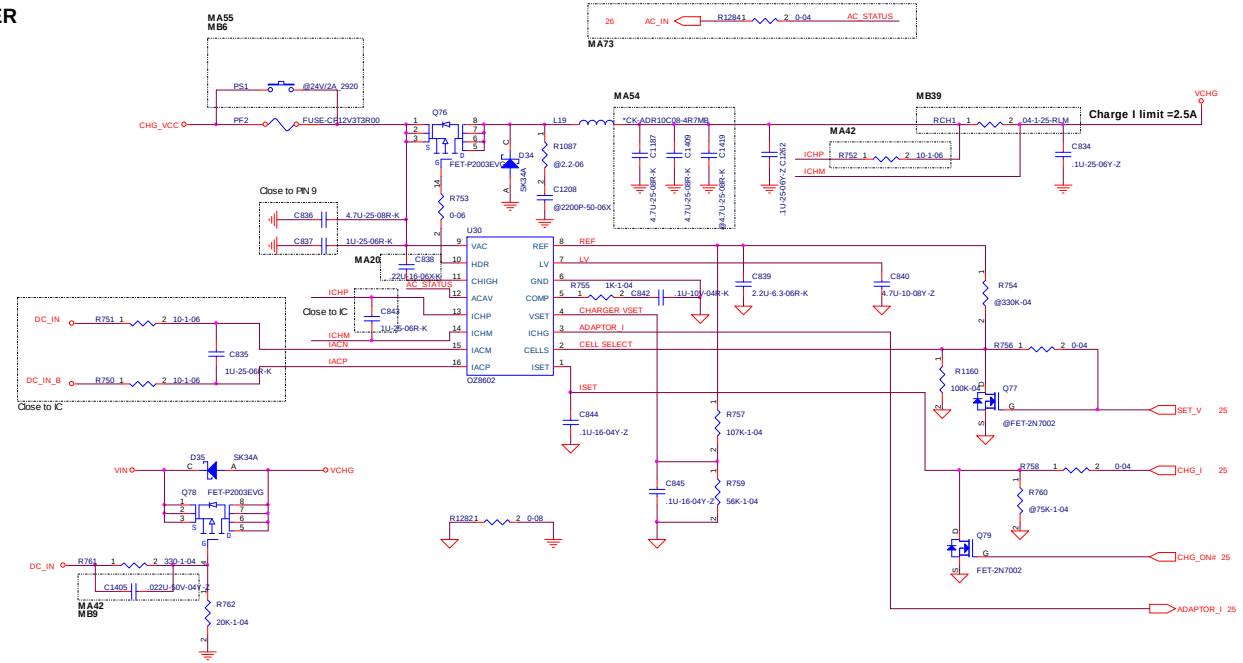
CHARGER



SET_V	
H	16.84V (4CELL)
L	12.71V (3CELL)

Vch =Nx(4.1 +Vset/10)
N=Cell (pin2 =high -->4, low -->3)

For Q77,R754 mount

SET_V	
L	16.84V (4CELL)
H	12.71V (3CELL)

CHG_I	Ich
3.36V	2.8A
3V	2.5A
2.4V	2A
1.2V	1A
0.48V	0.4A
0.3V	0.25A

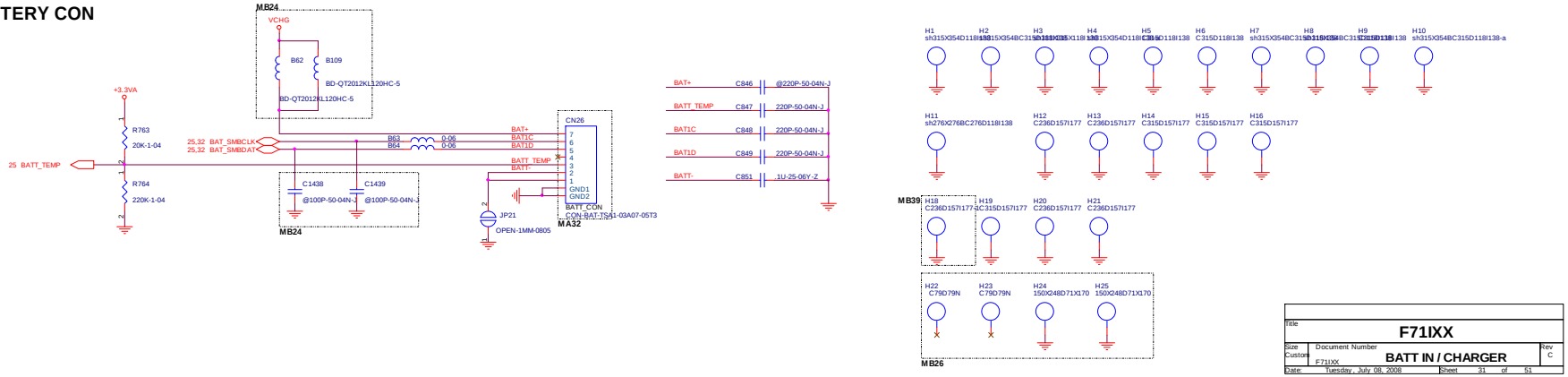
CHARGER CURRENT =V(CGH_I)/(Rch*30)

CHG_ON	
L	CHARGER_ON
H	CHARGER_OFF

ADAPTOR_I					
F50II0		F50IN0		F50IN5	
Voltage	W	Voltage	W	Voltage	W
330mV	20W	250mV	20W	180mV	20W
660mV	40W	500mV	40W	360mV	40W
990mV	60W	750mV	60W	540mV	60W
1.32V	80W	1V	80W	720mV	80W
X	X	1.25V	100W	900mV	100W
X	X	X	X	1.08V	120W

Vichg =RAD1*Irsense*10

BATTERY CON



Title	F71IXX
Size	Custom
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	BATT IN / CHARGER
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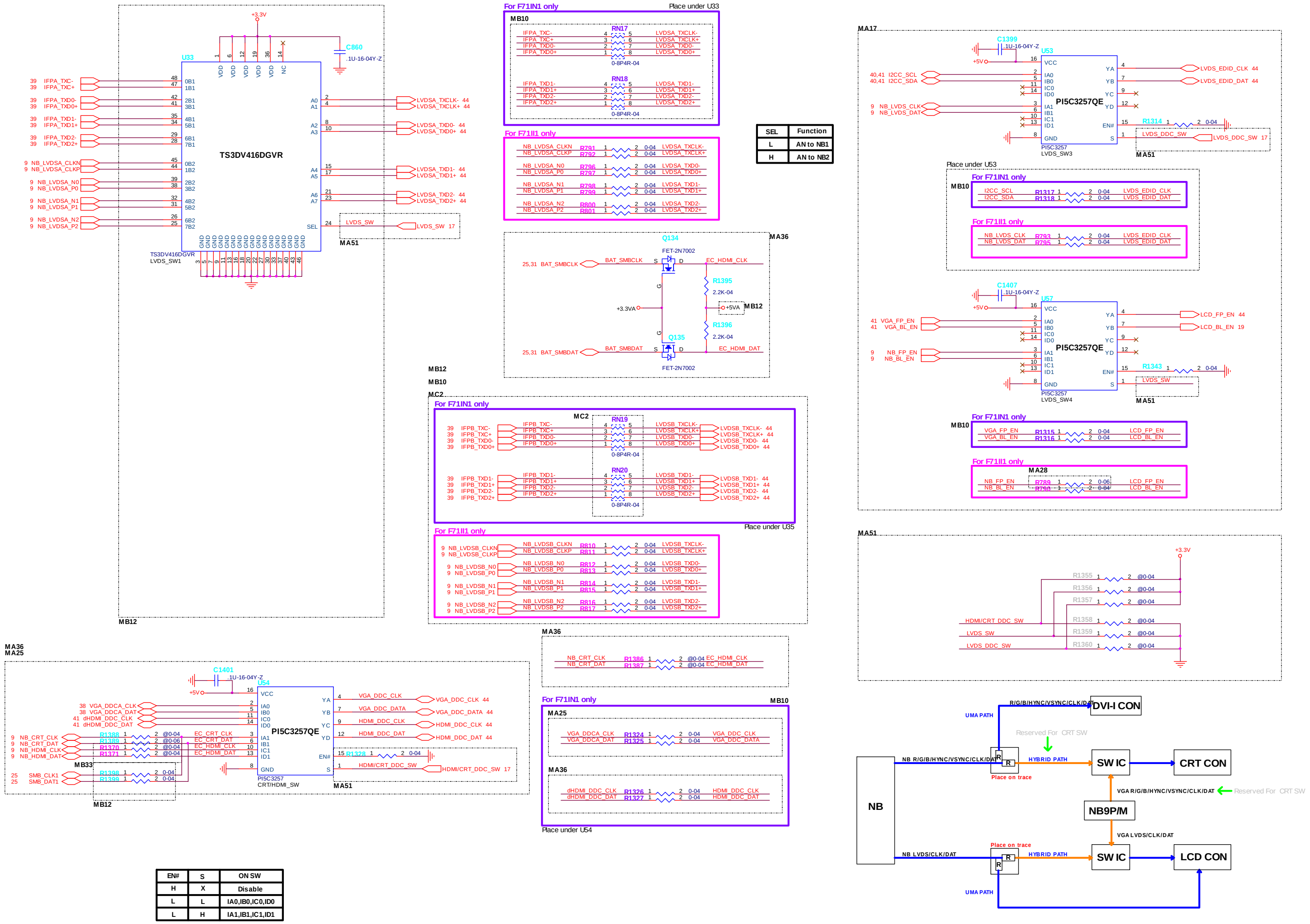

SEL	Function
L	AN to NB1
H	AN to NB2

EN#	S	ON SW
H	X	Disable
L	L	IA0,IB0,IC0,ID0
L	H	IA1,IB1,IC1,ID1

Title: F71IXX

Size: Custom | Document Number: F71IXX HYBRID SIGNAL SW | Rev: C

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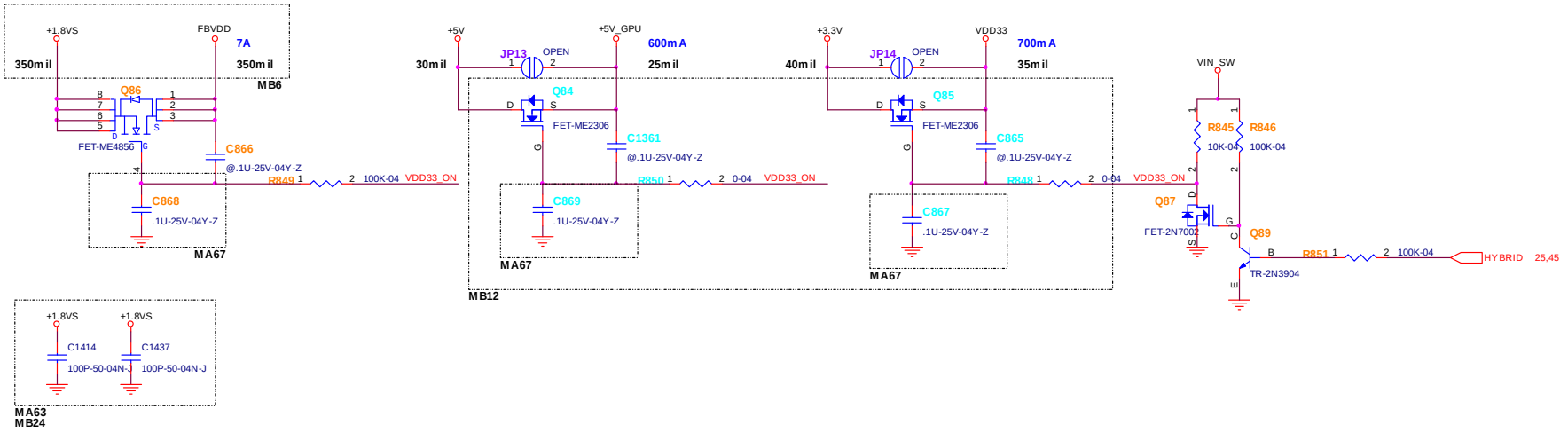
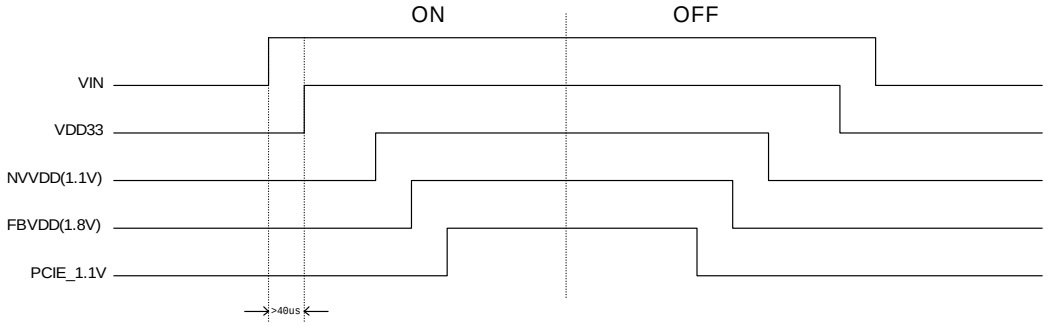


NB9P/M Power ON/OFF Sequence



Title	F71IXX	
Size: B	Document Number: F71IXX HYBRID POWER SW	Rev: C
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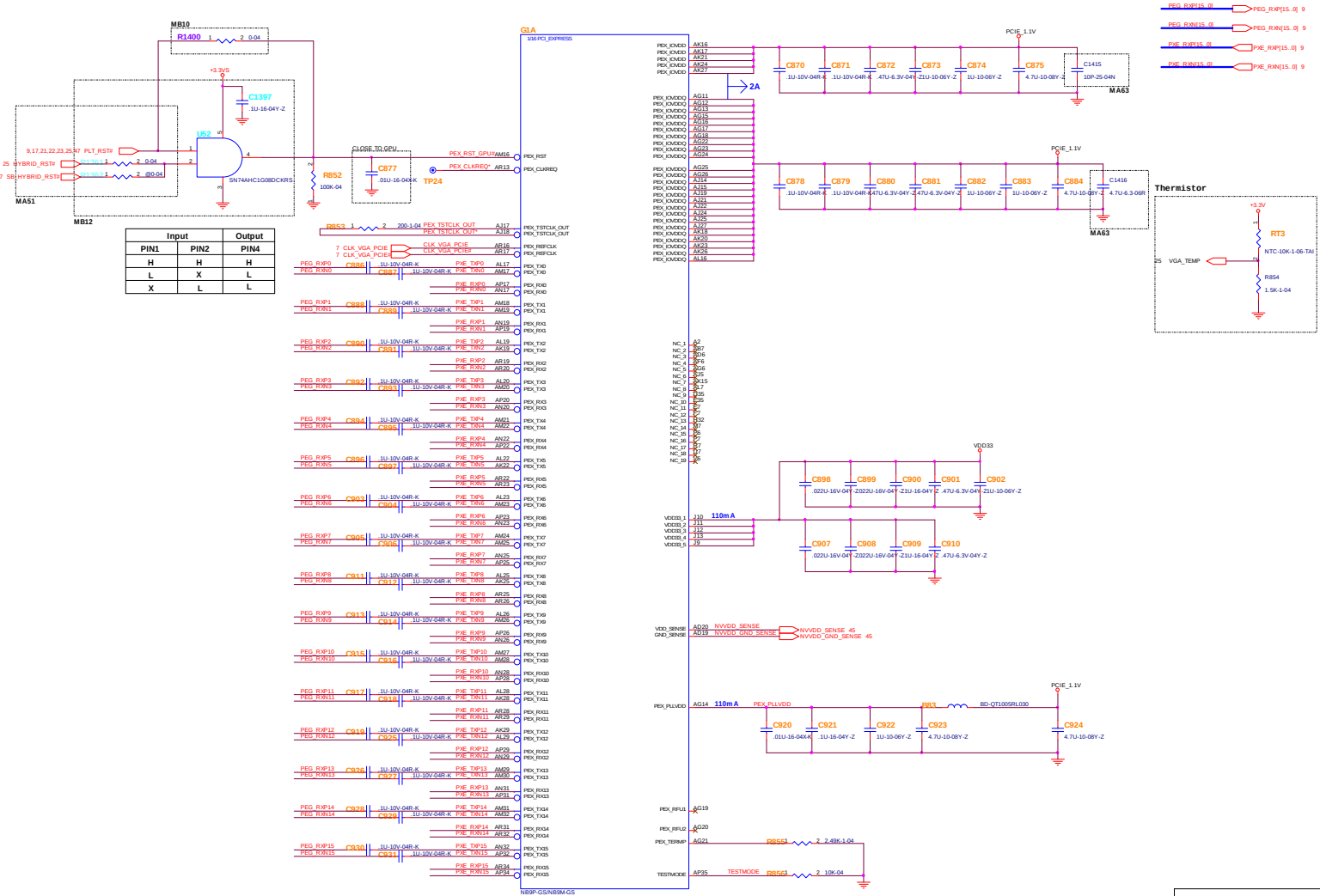

Input		Output
PIN1	PIN2	PIN4
H	H	H
L	X	L
X	L	L

Title	F71IXX
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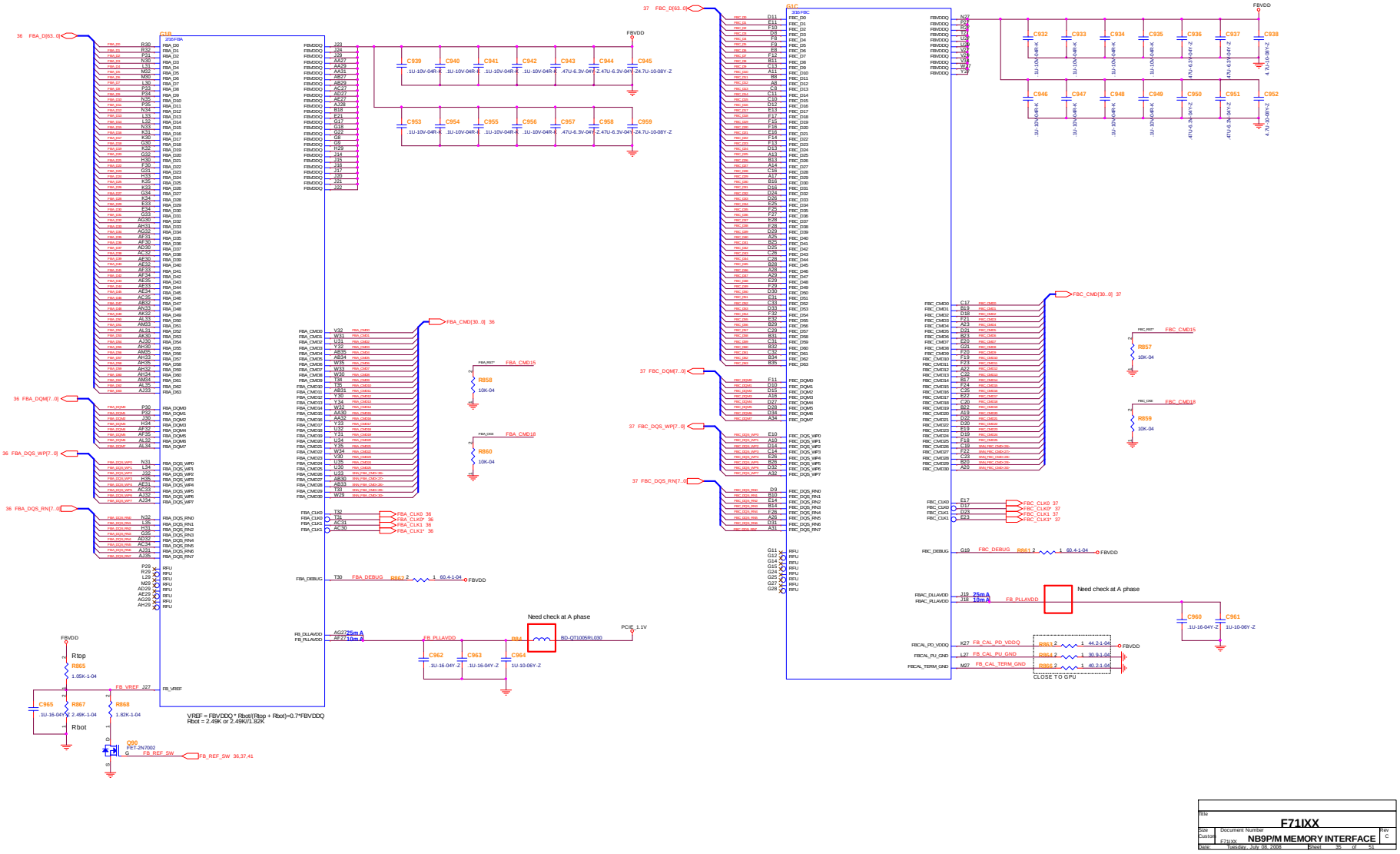

Title	F71IXX		
Size: Custom	Document Number: F71IXX	NB9P/M MEMORY INTERFACE	Rev: C
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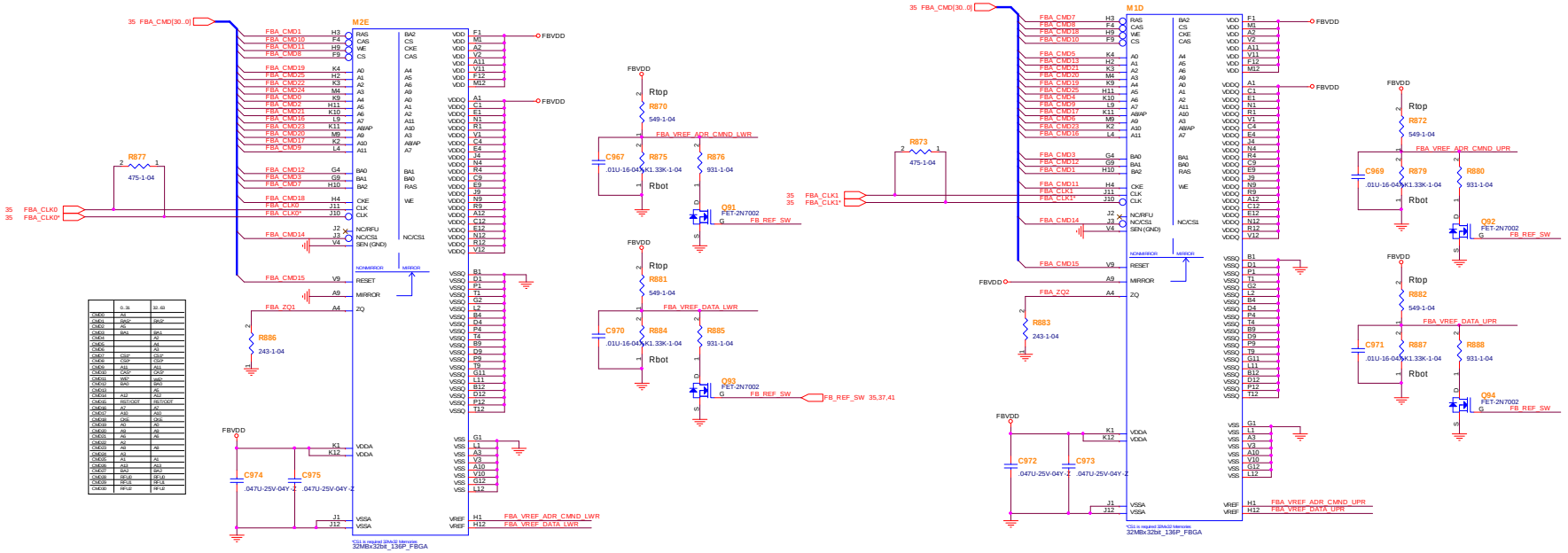
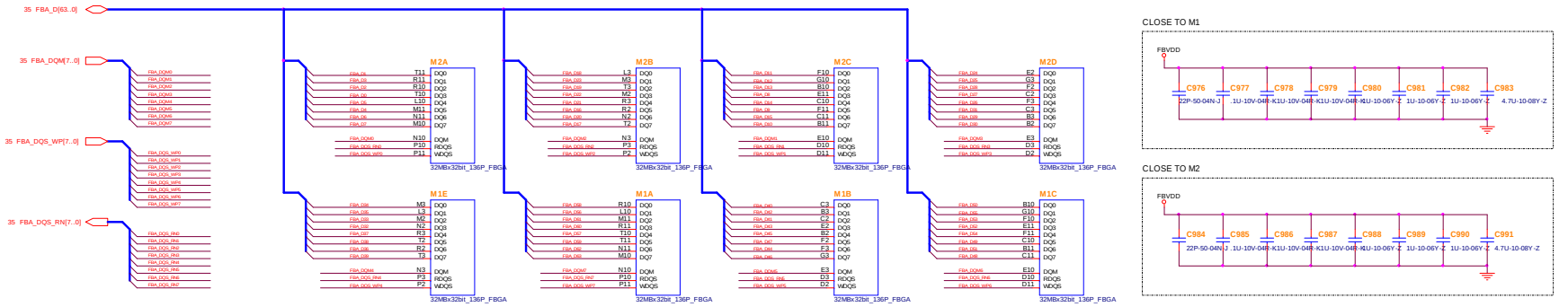


FBA MEMORY DECOUPLING



Title	F71IXX		
Size: Custom	Document Number: NB9P/M DDR3 16MX32 PART A		Rev: C
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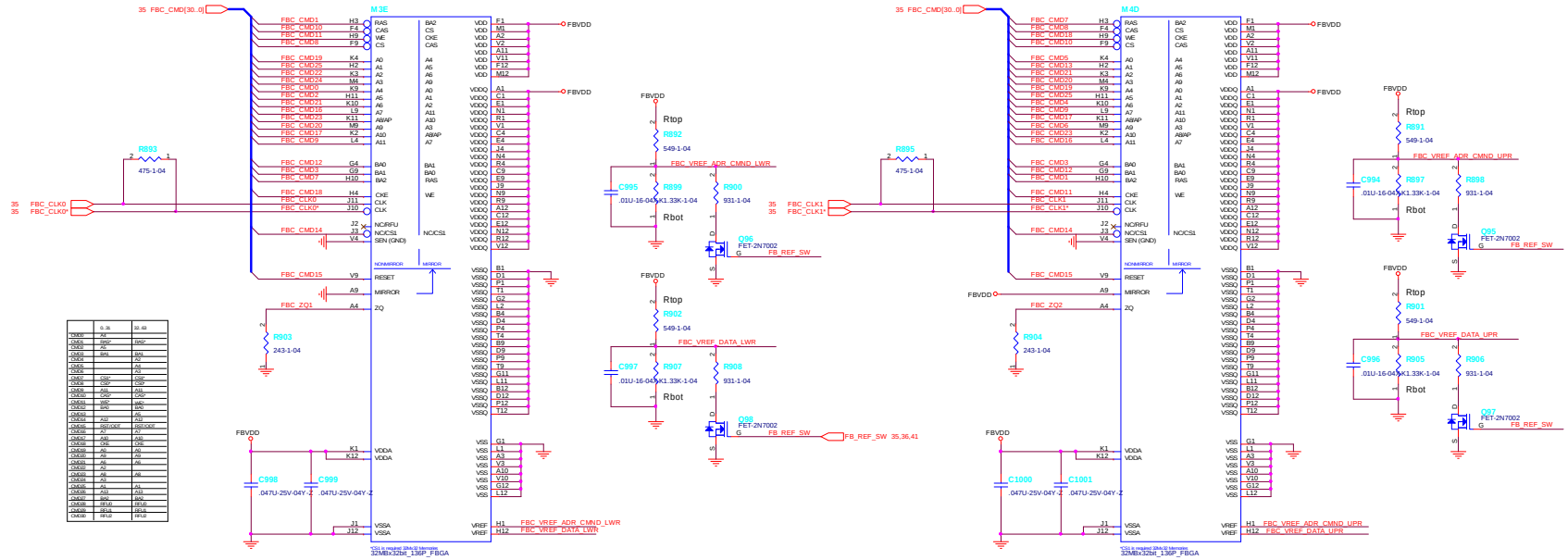
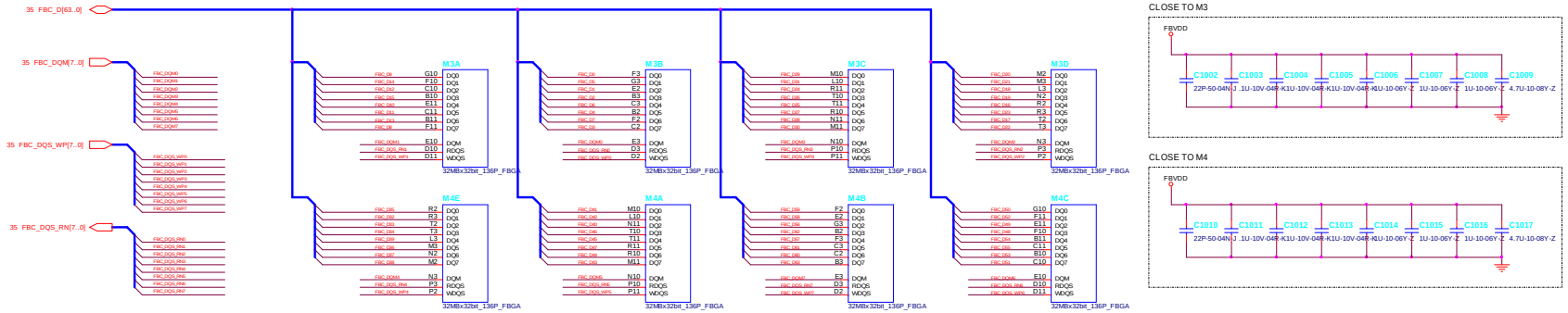


FBC MEMORY DECOUPLING



Title	F71IXX	
Size: Custom	Document Number: NB9P/M DDR3 16MX32 PART C	Rev: C
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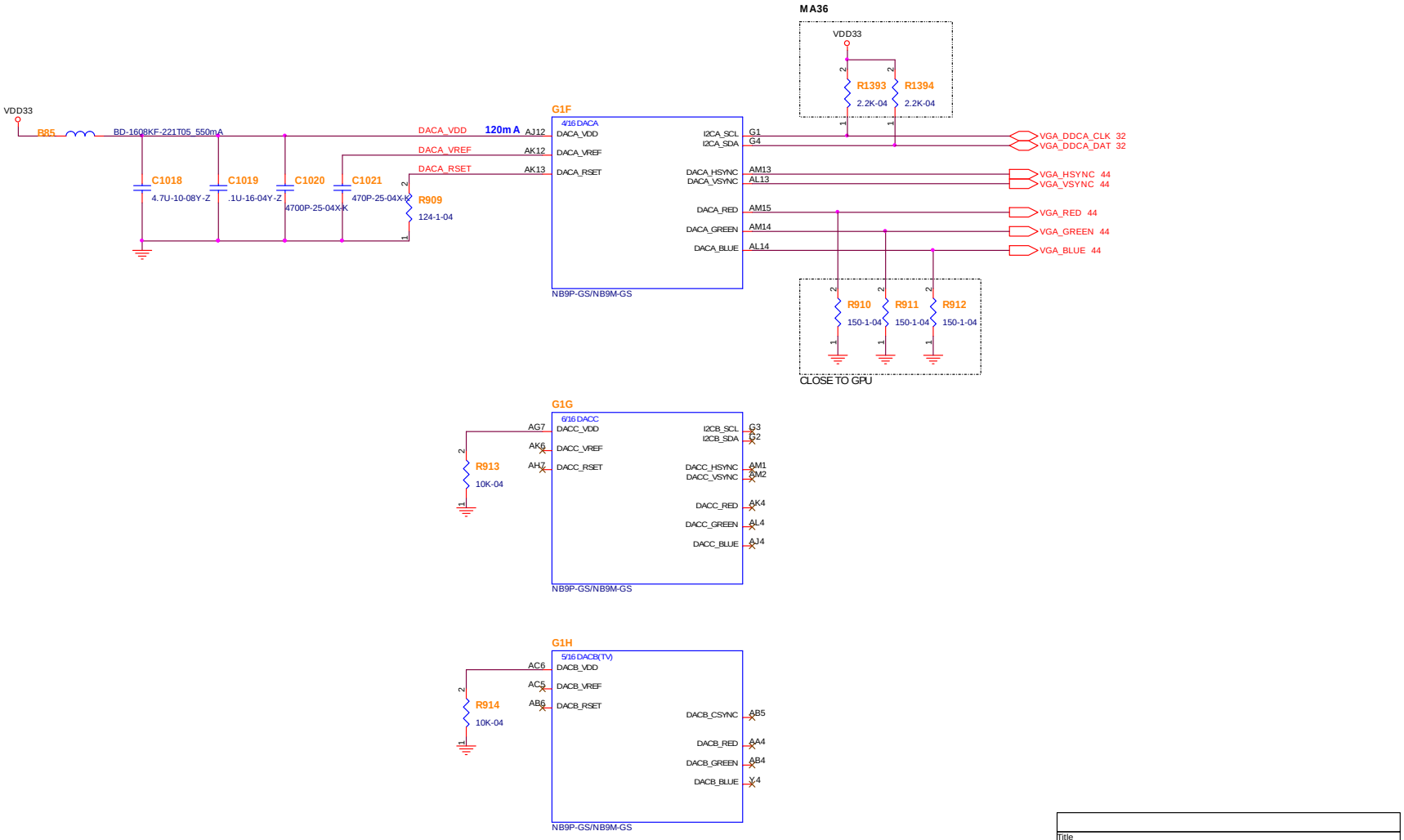

Title	F71IXX	
Size: B	Document Number: F71IXX NB9P/M DACA / DACB / DACC	Rev: C
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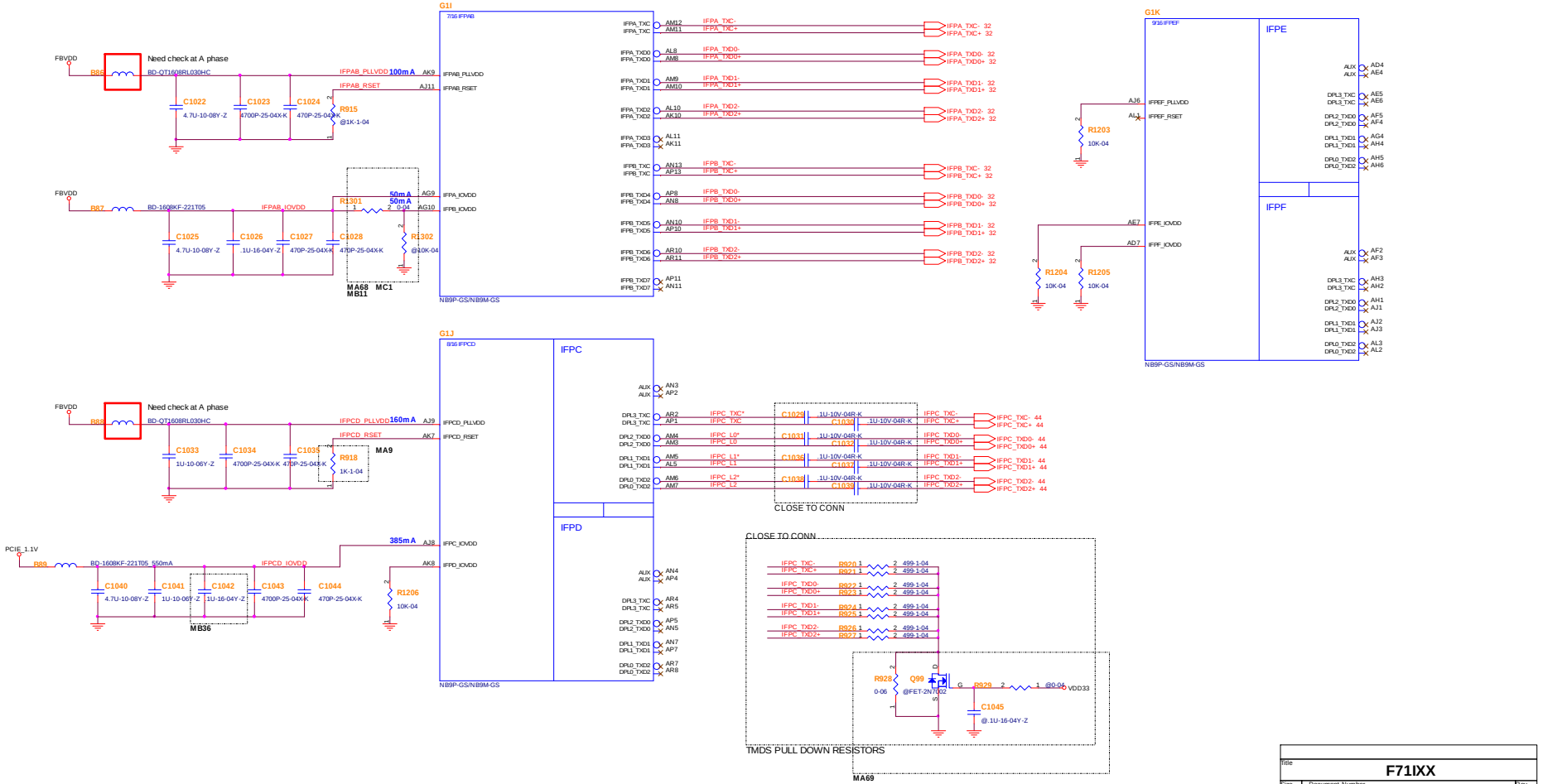

Title	F71IXX		
Size: Custom	Document Number: F71IXX	NB9P/M LVDS / TMDS	Rev: C
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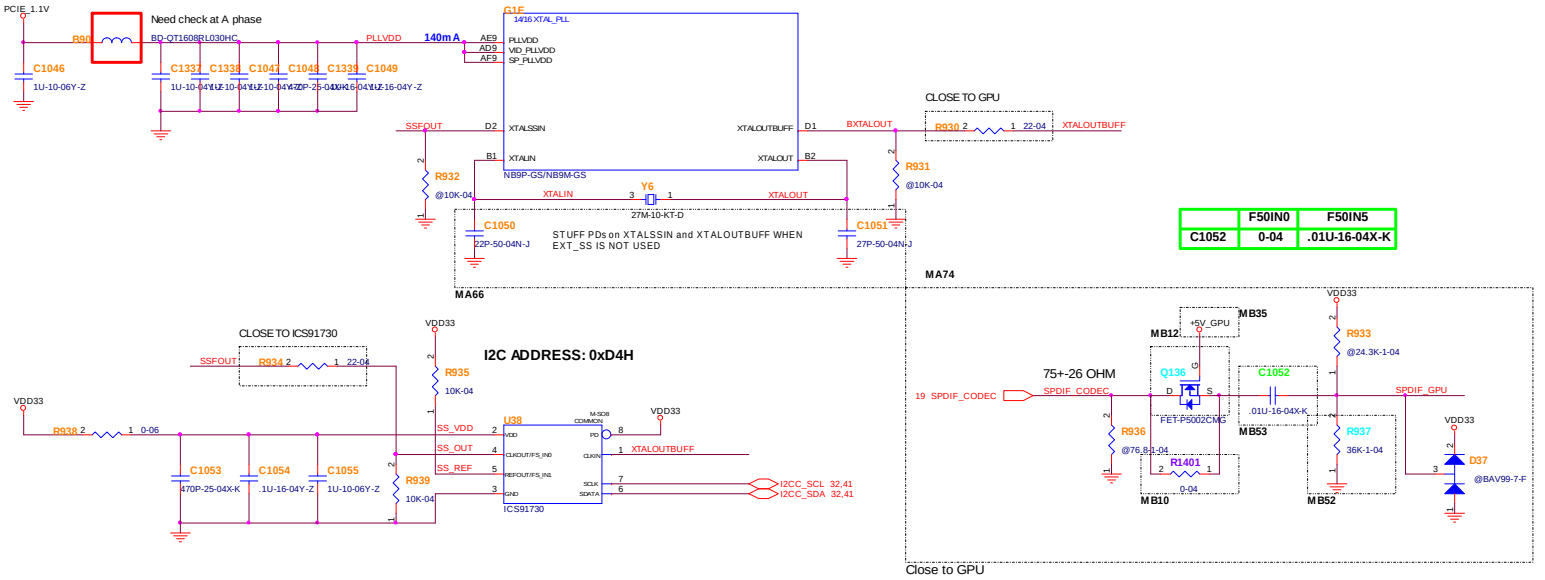

Title	F71IXX		
Size: Custom	Document Number: F71IXX	NB9P/M SS/BIOS/HDCP/XTAL	Rev: C
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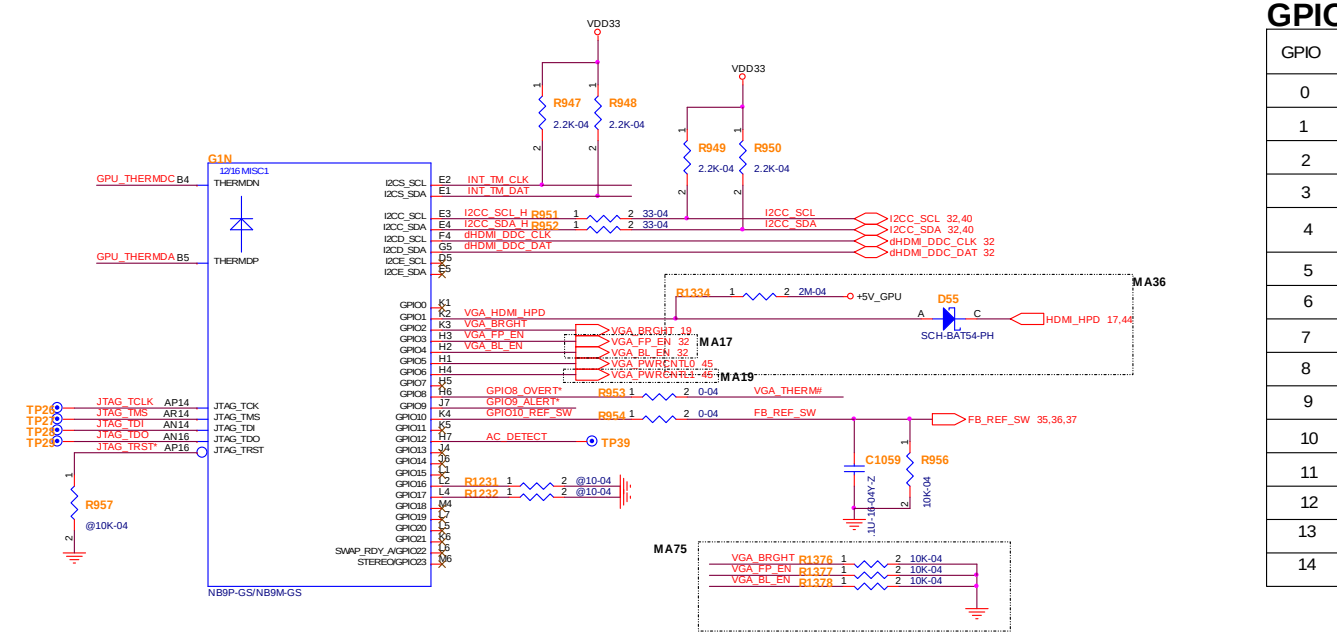
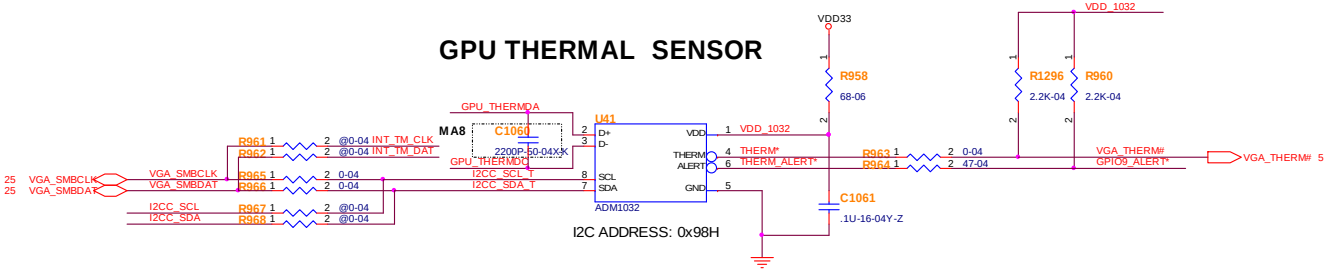


GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL

GPU THERMAL SENSOR



Title	F71IXX		
Size: Custom	Document Number: F71IXX	NB9P/M GPIO / THERMAL	Rev: C
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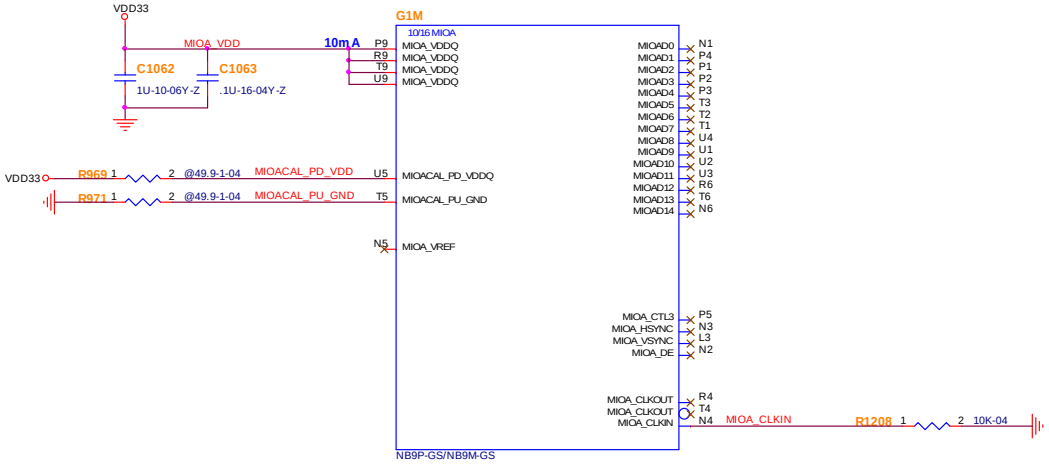
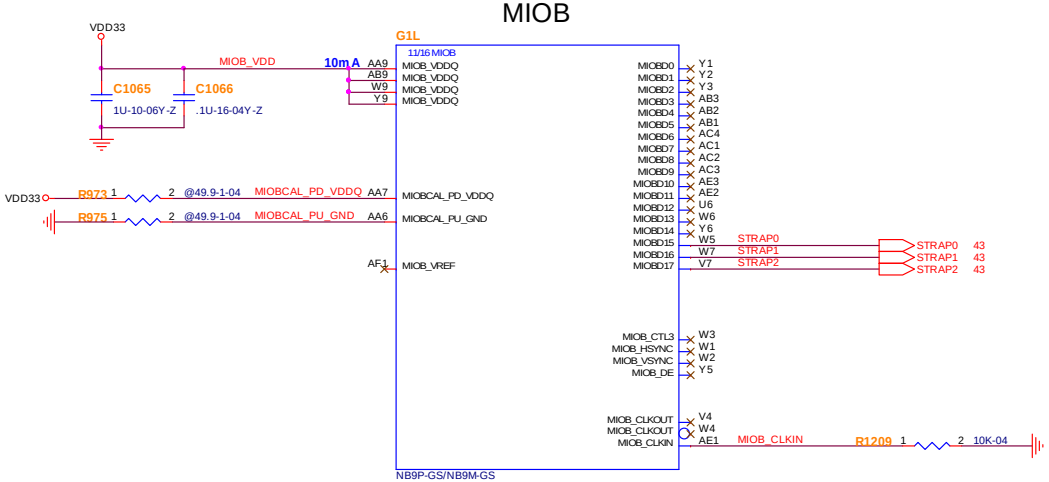
MIOA



MIOB



Title	F71IXX	
Size: B	Document Number: F71IXX — NB9P/M MIOA / MIOB	Rev: C
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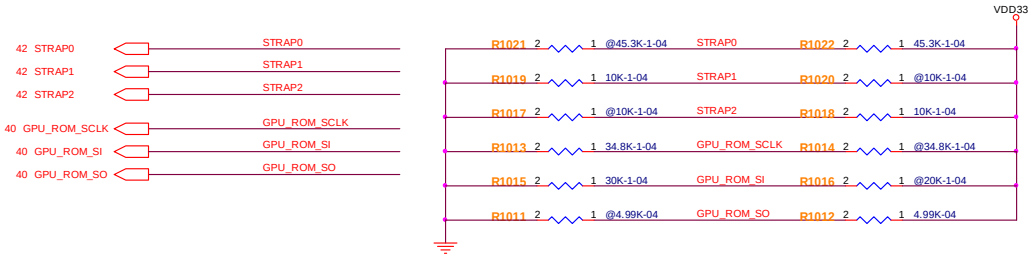

NB9M-GS/NB9P-GS

(GDDR3: Qimonda 16Mx32)

Strap[0] --> pull up 45K ohm 1% to +3VS
Strap[1] --> pull down 10K ohm 1% to GND
Strap[2] --> pull up 10K ohm 1% to +3VS
ROM_SCLK --> pull down 35K ohm 1% to GND
ROM_SI --> pull down 10K ohm 1% to GND
ROM_SO --> pull up 5K ohm 1% to +3VS

(GDDR3: Hynix 16Mx32)

Strap[0] --> pull up 45K ohm 1% to +3VS
Strap[1] --> pull down 10K ohm 1% to GND
Strap[2] --> pull up 10K ohm 1% to +3VS
ROM_SCLK --> pull down 35K ohm 1% to GND
ROM_SI --> pull down 15K ohm 1% to GND
ROM_SO --> pull up 5K ohm 1% to +3VS

(GDDR3: Samsung 16Mx32)

Strap[0] --> pull up 45K ohm 1% to +3VS
Strap[1] --> pull down 10K ohm 1% to GND
Strap[2] --> pull up 10K ohm 1% to +3VS
ROM_SCLK --> pull down 35K ohm 1% to GND
ROM_SI --> pull down 20K ohm 1% to GND
ROM_SO --> pull up 5K ohm 1% to +3VS

Signal	Bit 3	Bit 2	Bit 1	Bit 0
GPU_ROM_SO	1	0	0	1
GPU_ROM_SCLK	?	1	1	1
GPU_ROM_SI	0	0	0	1
STRAP2	1	0	0	1
STRAP1	0	0	0	1
STRAP0	1	1	1	1

Title	F71IXX	
Size: Custom	Document Number: F71IXX NB9P/M STRAP	Rev: C
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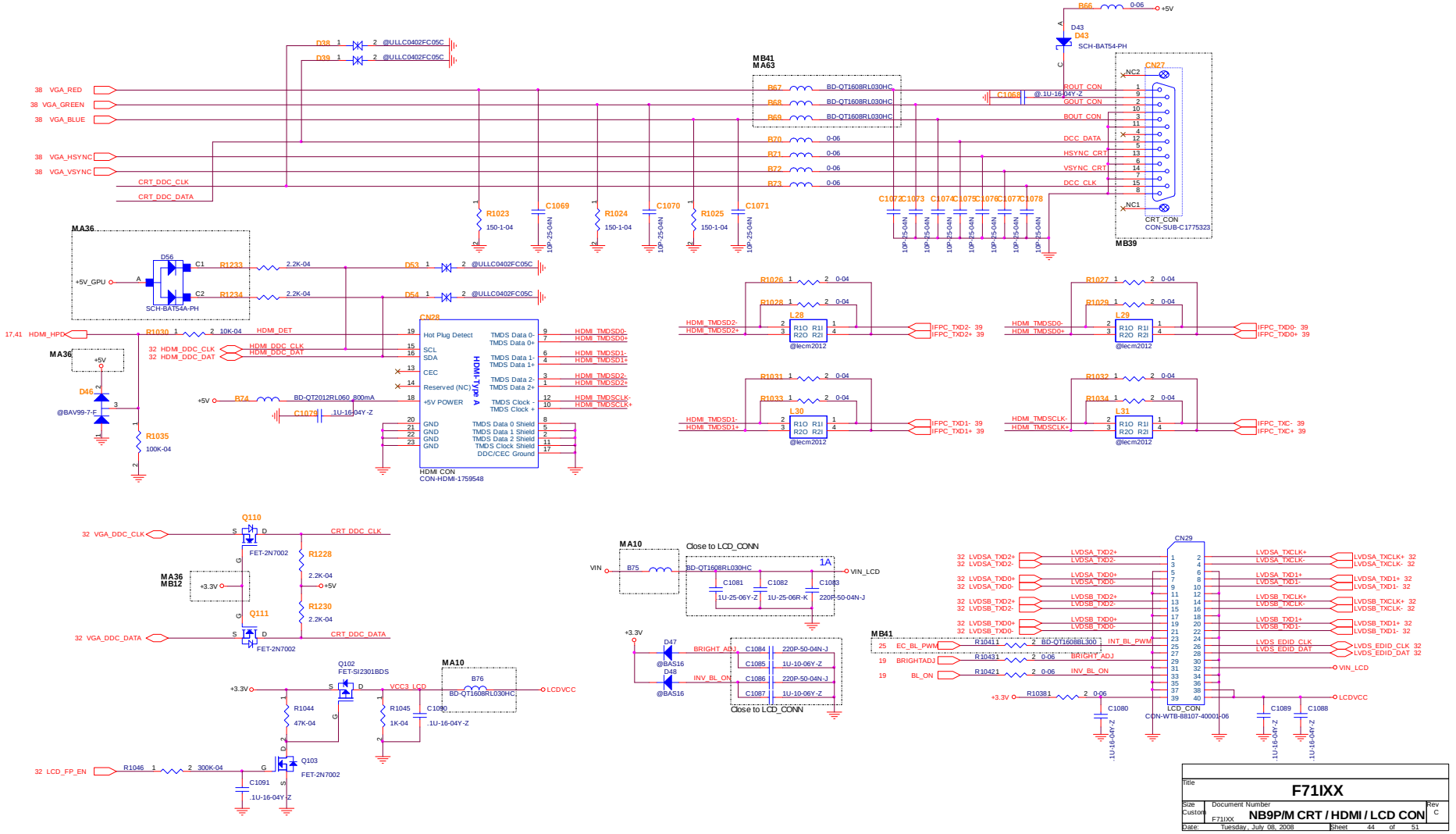

Title	F71IXX		
Size: Custom	Document Number: NB9P/M CRT / HDMI / LCD CON		Rev: C
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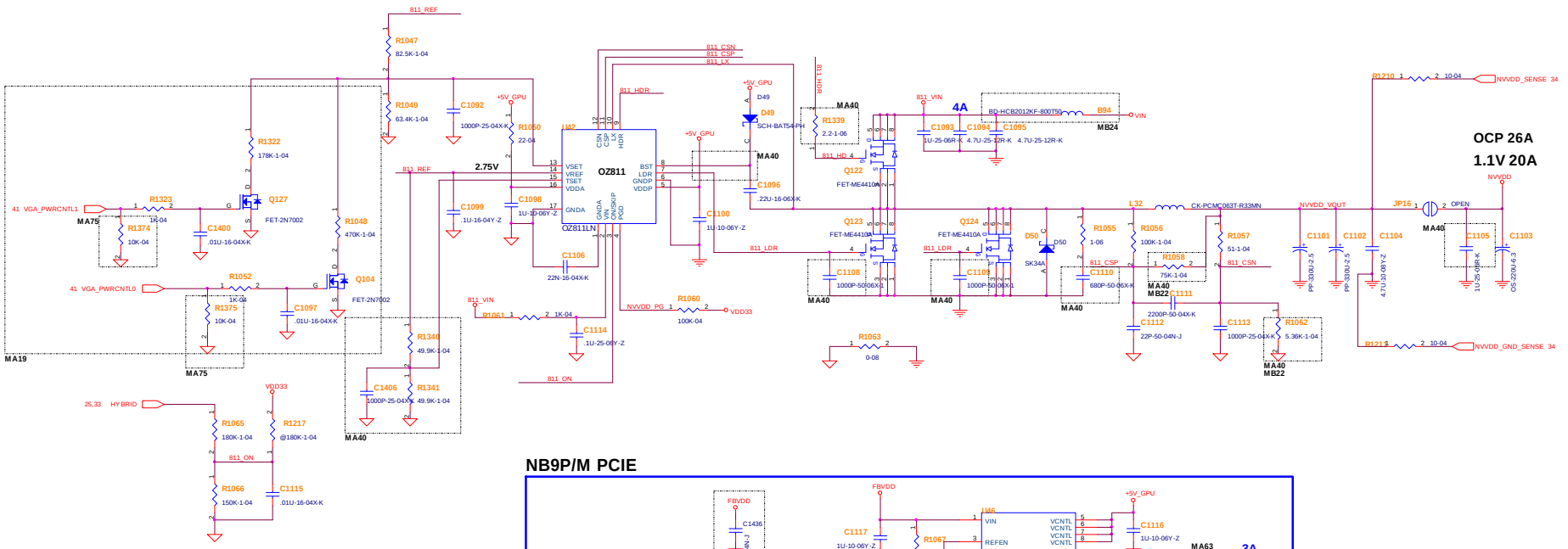
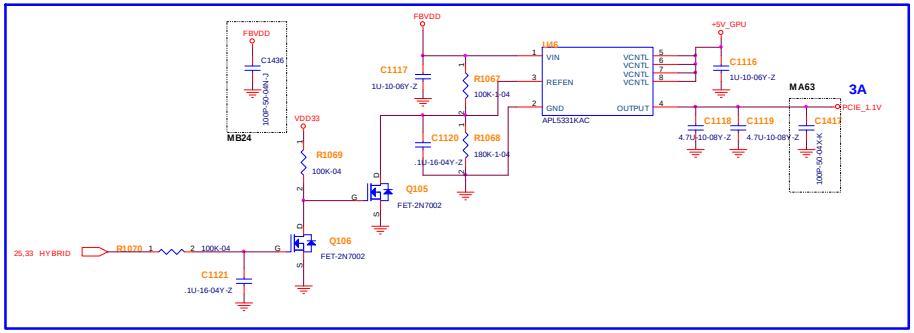


NB9P/M PCIE



ITEM		NB9M-GS			NB9P-GS		
POWER SETTING		Performance	Balance	Max Bat	Performance	Balance	Max Bat
VGA_PWRCNTL0		L	L	L	H	H	H
VGA_PWRCNTL1		L	L	H	L	L	H
VOLTAGE		1.17V	1.17V	0.95V	1.05V	1.05V	0.9V
E/M CLOCK (With Loading)	AC	580/700	580/700	275/300	500/800	500/800	275/300
	DC	580/700	580/700	275/300	500/800	500/800	275/300
E/M CLOCK (Idle)	AC/DC	169/100					

Title	F71IXX		
Size: Custom	Document Number: F71IXX	NB9P/M NVDD / PCIE1.1V	Rev: C
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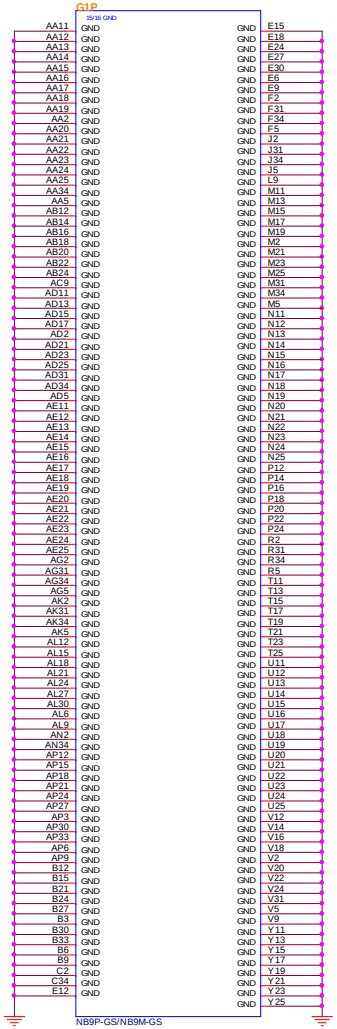

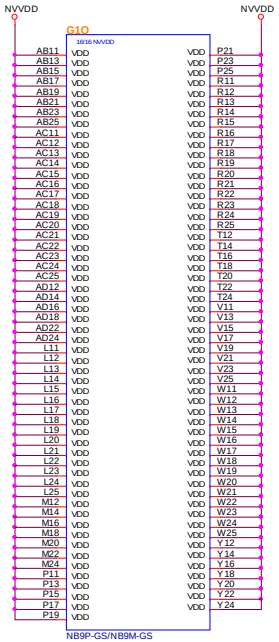

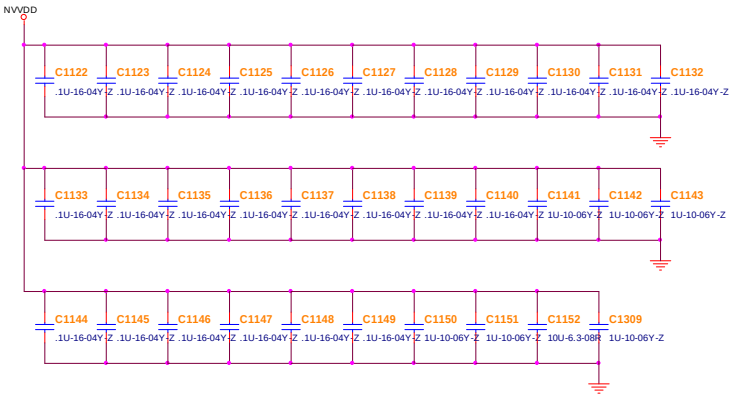

Title	F71IXX	
Size: Custom	Document Number: F71IXX NB9P/M NVVDD/DECOUPLING CAP	Rev: C
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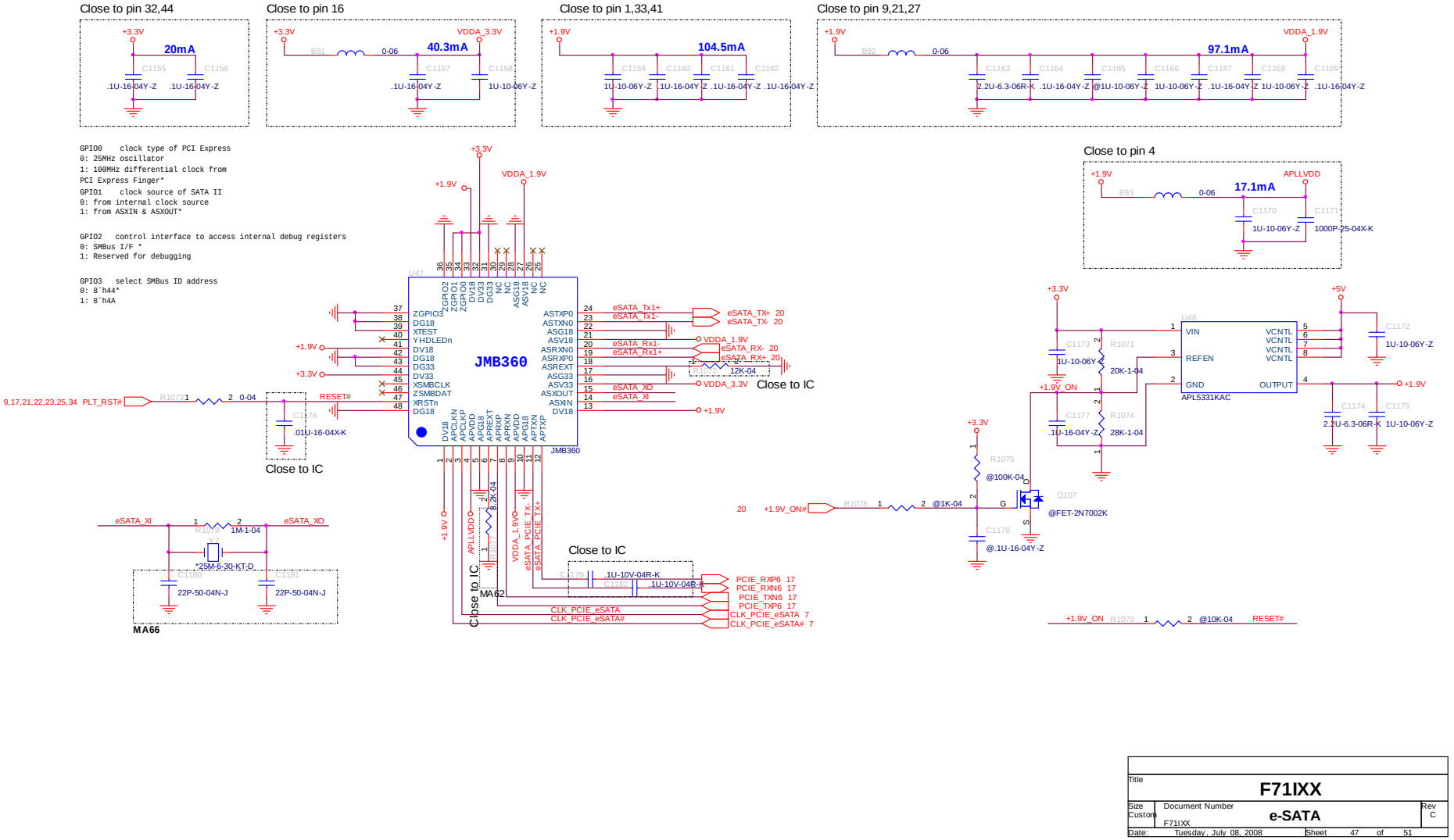

Title	F71IXX		
Size: Custom	Document Number: F71IXX	e-SATA	Rev: C
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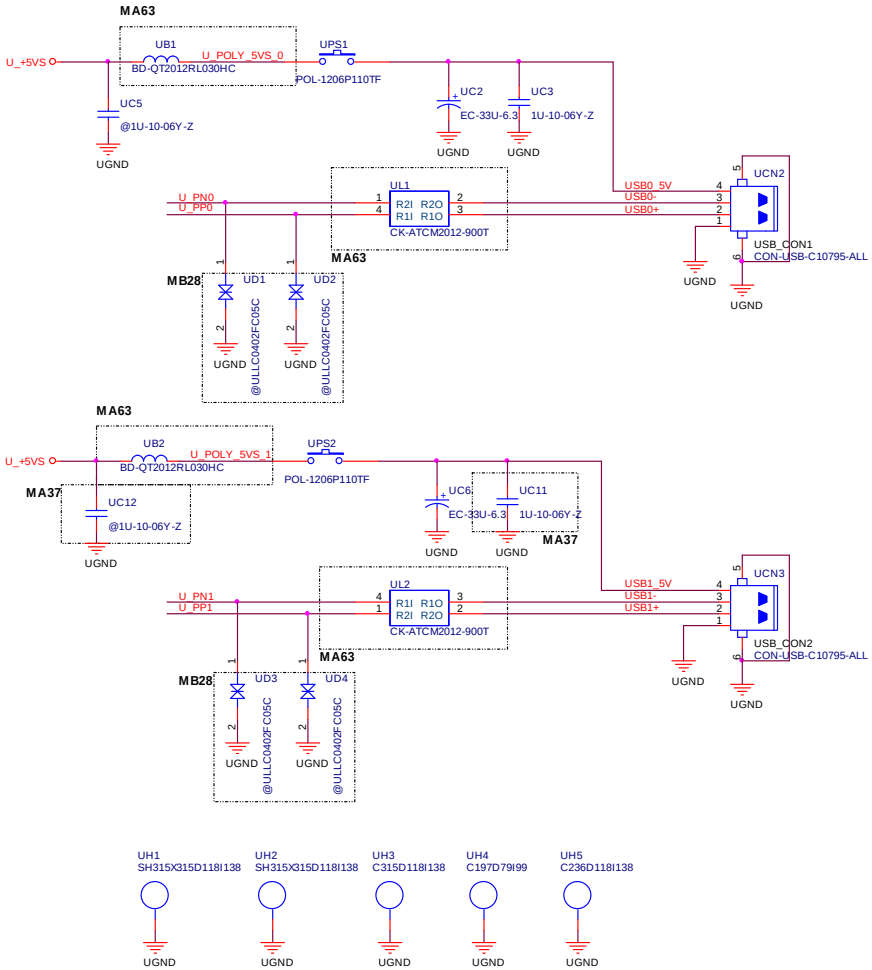
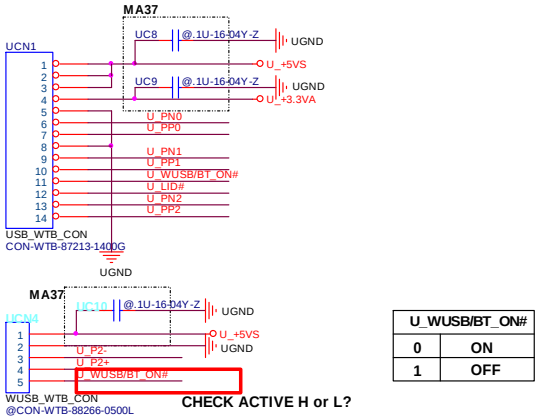
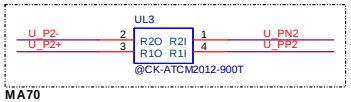
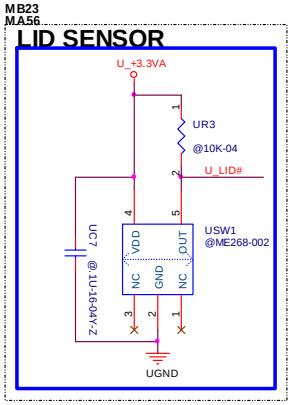




U_WUSB/BT_ON#	
0	ON
1	OFF





PCB P/N : 35GEF5000-C0
PCBA P/N : 80GEF5000-C0

Title	F71IXX		
Size B	Document Number F71IXX	USB BD	Rev C
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RA to RB Modify list:

Symbol	Modify Item	Modify Reason	Page	Note
MA1	S1 correct footprint to 1206 package	Footprint error	20	
MA2	CN15 correct layout library	Library error	20	
MA3	C783,C1242 change footprint to 0402 package	To avoid interfere with system memory	29	
MA4	C276,C277 correct footprint to 0402 package	Footprint error	12	
MA5	Change net name from TBD# to BROWSER#	FSC spec confirm BROWSER#	19,25	
MA6	ADD R1307,R1308,R1309,R1310 Add R1311	Reserved for disable TV/CRT function when use Hybrid function	9,11	
MA7	Change R490 from 100K-1-04 to 1K-1-04	Fan can' work due to bom error	24	
MA8	Change C1060 from @2200P-50-04X-K to 2200P-50-04X-K	Reduce thermal sensor noice	41	
MA9	Change R918 from @1K-1-04 to 1K-1-04	For NB9P/M HDMI function	39	
MA10	Change B75,B76 from BD-QT2012RL030HC_3A to BD-QT1608RL030HC	Bom error	44	
MA11	Change C806,C807 to 0805 package	Footprint error	29	
MA12	NB_CRT_R and NB_CRT_B swap	Net error	15	
MA13	Change R189 from 20K-1-04 to 43.2K-1-04 Change R214 from 10k-04 to 10K-1-04	For DDC_EN input Level	14,15	
MA14	Change R203,R206,R209,R210 to 68-1-04 Change C342,C343,C344,C345 from 0-04 to 1P-50V-04N-C	For CH7318 DVI function	14	
MA15	CLK_ICH_SATA and CLK_ICH_SATA# swap	Net error	16	
MA16	Add R1312,R1313 10K-04 pull up	Follow Intel comments for ICH9M USB OCP	17	
MA17	Add U53,U57,Q130,R1314,R1315,R1316,R1317,R1318R1343,R1344,R1345,C1399,C1407,C1048	For LVDS Hybrid DDC/Control signal	32,47	
MA18	Change U40 to I2CROM Add R1319,R1320,R1321 Change R944 from 10K-04 to @10K-0 ; R1207 from @10K-04 to 10K-04	1.For NV change HDCP ROM from Crypto ROM to I2C ROM 2.Colayout Crypto ROM and I2C ROM	40	
MA19	Add VGA_PWRCNTL1 Add Q127,R1322,R1323 R1049 change from 56-1-04 to 63.4K-1-04 ,R1048 change from 210K-1-04 to 470K-1-04	Follow NV GPU core spec	41,45	
MA20	Change C838 from .47U-25-06Y-Z to .22U-16-06X-K	For sourcer request to solve shortage issue	31	
MA21	Change R377,R378 from 100K-04 to 4.7K-04	For SMBUS pull high level	19	
MA22	Change R707 from 90.9K-1-04 to 97.6K-1-04	Solve F50IN0 3D MArk'6 can't run due to 1.8V voltage level too low for GPU	29	
MA23	Change R686 to from 54.9K-1-04 to 62K-1-04	System sometimes will blue screen due to 1.05V voltage level too low for NB	29	
MA24	Change R1247,R1270 from 2.1K-1-04 to 1.15K-1-04 Change R1255,R1272 from 4.02K-1-04 to 649-1-04 Change R1303,R1304 from 4.02K-1-04 to 0-04	System abnormal shutdown due to Vcore OCP setting too low	27	
MA25	Add U54,R1324,R1325,R1328,C1401	For CRT Hybrid function support	32	
MA26	Add KEY_OUT1/KEY_OUT17	Reserved for 17" keyboard number pad	25	
MA27	Reserved R1329,C1402 for ITE8512-JX	ITE8512IX will phase out	25	
MA28	R789,R1143,R124,R125,R408 change package from M-R0402 to M-R0603 Change R1111 from 0-08 to 0-06	For layout require	9,30 13	
MA29	R124,R125 change from option to mount for all project	For CRT Hybrid DDC detect	9	
MA30	Change C358,C362 from 1U-10-06Y-Z to @1U-10-06Y-Z ;change C359,C363 from 1U-10-06Y-Z to .22U-16-06X-K	For RTC_RST# Rising time	16	
MA31	Change U49 footprint from M-SOP8B to M-SO8	Footprint error	17	
MA32	Change CN26 footprint from con_bat-m7_btj-07ro4g-sd001_oct to C144F3-X07XX-X	For M1 request	31	
MA33	Change R273 from 0-04 to @0-04	Schematic error , for Keep CPU clock output when system entry C3	17	
MA34	Remove R1099 and del net VL	Doesn't need for U18	28	
MA35	Change C1214,C1209 from .1U-16-04Y-Z to .01U-16-04X-K	Reduce +3.3VA_ON/+5VA_ON noise	28	
MA36	Add Q128,Q129,Q134,Q135,Q137,D55,D56,R1326,R1327,R1370,R1371,R1384,R1385,R1390, R1393,R1394,R1386,R1387,R1388,R1389 and del R1227,R1229 Reserved R1334 and change R205 setting	For HDMI Hybrid DDC detect For HDMI Hybrid HPD detect	9,32,41	
MA37	Change C1305,C1306,C1307,C1185,C1186 to UC9,UC10,UC8,UC11,UC12	Correct location name error	48	
MA38	Add R1335,R1336,C1403 and del R1102,R1104 Change C1220,C1237 from @3300P-50-06X-K to 3300P-50-06X-K Change R1096,R1109 from @2.2-06 to 1-06 Change C1221,C1236 from @2200P-50-06X to 560P-50-06X-K Change C1234 from @470P-50-06N-K to .01U-50V-06Y-Z and C1235 from 470P-50-06N-K to .01U-50V-06Y-Z Change R1100 from 40.2K-1-04 to 147K-1-04 and R1112 from 40.2K-1-04 to 100K-1-04	Improve 3/5V power quality	28	
MA39	Add R1337,R1338,C1404 and del R697,R699 Change C773,C774 from @3300P-50-06X-K to 3300P-50-06X-K Change C794,C795 from @3300P-50-06X-K to 2200P-50-06X Change R692,R704 from @2.2-06 to 1-06 Change C775,C796 from @2200P-50-06X to 560P-50-06X-K and 1000P-50-06X-1 Change R695,R708,C776,C797 to option Change C776,C797 from 6800P-50-04X-K to 8.2N-25-04X-K	Improve 1.05/1.8V power quality	29	
MA40	Add R1340,R1341,C1406,R1339 and del R1051 Change C1108,C1109 from @2200P-50-06X to 1000P-50-06X-1 Change C1110 from @3300P-50-06X-K to 680P-50-06X-K Change R1058 from 100K-1-04 to @100K-1-04 Change R1062 from 5.6K-1-04 to 11.5K-1-04	Improve GPU 1.1V power quality	45	
MA41	Change R347 from 22.6-1-04 to 20-1-04	Improve USB signal quality	17	
MA42	Add C1405 Change R752 package from M-R0402 to M-0603	To protect battery when AC IN To enhance current rating for net "ICHP"	31	
MA43	Add net "AUX_PWR_EN"	correct Aux power enable function under AC mode	26,28	
MA44	Add R1346,R1347 Shift net from PIN32~PIN40	For EMI request	17	
MA45	Add R1348	To disable iTPM	25,32	
MA46	Change R356,R357 from 0-06 to @0-06 Change C1320,C1321 from .1U-10V-04R-K to @.1U-10V-04R-K	VCCSUS1_05 and VCCSUS1_5 power are internal output don't need external power supply	18	
MA47	Change R330,R301,R262,R263 from 10K-04 to @10K-04	Follow Intel schematic	17	
MA48	Correct power plane from +3V to +3VS	Net error	17	
MA49	Reserved R1349	For ODD detect	20	
MA50	Change LAN_PHYPC from GPIO8 to GPIO12	Net error	17	
MA51	Del Q83,R820,R830,C1391 Reserved R1355,R1356,R1357,R1358,R1359,R1360 Add R1350,R1351,R1352,R1353	Change Hybrid SW control signal from EC to SB	17,25,32	
MA52	Change R41 from @10K-04 to 100K-04 Change +3.3V to VDD_7421	Reserved pull high for NS For thermal IC power sequence	5	
MA53	Change R52 from 10K-04 to 1.5M-04 Add C1408,R1363	improve clkgen intial time	7	
MA54	Add C1409,C1419 and del C833	Reduce charger power noise	31	
MA55	Reserved PS1,JP26	For safety request	31	
MA56	Change R1299 from 0-04 to @0-04 Change C470 from .1U-16-04Y-Z to 0-04 Change UR3 from 10K-04 to @10K-04 Change UC7 from .1U-16-04Y-Z to @.1U-16-04Y-Z Change USW1 from MLX90248 to @MLX90248 Change R537 from @4.7K-04 to 4.7K-04	Disconnect LID# path on USB BD	19,25,48	
MA57	Change R255 from 24.9-1-04 to 22.6-1-04	Improve SATA signal quality	16	
MA58	Change R482 from 10K-1-04 to 8.2K-1-04 Del R479,R480 Change R477,R478 from 10K-04 to 4.7K-04 Change R473 from 10K-04 to @390K-04 Add R1364,R1365,R1366	Follow Jmicro comments for 1394 only	23	
MA59	Del R143 and change net "PEG_RXPP3" to "PEG_RXP3"	Reduce PCIE signal branch	9	
MA60	Del R64	Use Crystal 12MHz to replace clockgen 48MHz For cardreader to improve EMI	7	
MA61	Change C1350 from @1000P-25-04X-K to 1000P-25-04X-K Change R298 from @100K-04 to 100K-04 Changr R1244,R1271 from 0-06 to 2.2-1-06 Changr C1348,C1357 from @1000P-25-04X-K to 3300P-50-06X-K	Improve Vcore power quality	17,27	
MA62	Change R1077 from 10K-1-04 to 8.2K-1-04	Value error	47	

MA63	Add C1410
	Change B29,B30,B31 from 0-06 to BD-QT1608RL060
	Change B42 from 0-08 to BD-QT2012RL030HC;del R405,R406
	Del C1380,C1387,C1388 and change C1379 C1381,C1382,C1393 from .1U-25V-04Y-Z to @100P-50-04X-K
	Add B102,B103,B104 and remove JP9
	Add C1412,C1413
	Add C1414
	Add C1415,C1416 for all project
	Change B67,B68,B69 from 0-06 to BD-QT1608RL060
	Add C1417
	Change UB1,UB2 from 0-08 to BD-QT2012RL030HC
	Del UR1,UR2,UR4,UR5
	Add C1421,C1422,C1423
	Del net "CLK_CARD48"
	Change R1297,R1298 from 0-06 to BD-QT1005RL030
	Change B11,B13,B15,B21 from 0-06 to BD-QT1608RL030HC
	Add B80 to option table
	Add B105 and change B57 from BD-4532KF-800T80 to BD-HCB2012KF-800T50
		For EMi request	13
			15
			20
			24
			29
			30
			33
			34
			44
			45
			48
			
			24
			19
			15
			11
			22
			26	

MA64	Add Q133,R1367,R1368,R1369 Add net "PWR_LED"	Improve power on LED light speed	19,25	
MA65	Correct VGA thermal sensor and dHDMI pull high power plane	Net error	25	
MA66	Change C102 from 20P-50-04N-J to 33P-50-04N-J Change C608,C609 from 20P-50-04N-J to 22P-50-04N-J Change C1050 from 18P-50-04N-J to 22P-50-04N-J and C1051 from 18P-50-04N-J to 27P-50-04N-J Change C1180,C1181 from 10P-25-04N to 22P-50-04N-J	Fine turn crystal accurate	7 23 40 47	
MA67	Change C1249,C1250,C1251,C1254,C1255,C1258,C1259,C867,C868,C869 from .1U-16-04Y-Z to .1U-25V-04Y-Z	Bom error	30	
MA68	Change R1301 from @0-04 to 0-04 and R1302 from 10K-04 to @10K-04	For LVDS B channel power supply	39	
MA69	Change Q99 from FET-2N7002 to @FET-2N7002 Change R928 from @0-06 to 0-06 Change R929 from 0-04 to @0-04 Change C1045 from .1U-16-04Y-Z to @.1U-16-04Y-Z	Change TMDS pull down path	39	
MA70	Del C75 Del UR6,UR7	For M1 requirement	7	
MA71	Change C466,C467 from @.1U-16-04Y-Z to .1U-16-04Y-Z	Reduce power noise	19	
MA72	Change R549 from 1K-04 to @1K-04 and update platform ID table	update plateform ID table	25	
MA73	Change R590 from 120K-1-04 to @120-1-04 and change R1306 from @0-04 to 0-04 Change R1284 from @0-04 to 0-04 Change R584 from 0-04 to @0-04 and change Q42 from FET-2N7002 to @FET-2N7002	Change ADAP_IN path to OZ8602	26 31	
MA74	Add Q136	For Hybrid audio	40	
MA75	Add R1374,R1375,R1376,R1377,R1378	For GPU GPIO pull down	41,45	
MA76	Add C1424,C1425	Reserved for ESD	16,17	

RB to RC Modify list:

Symbol	Modify Item	Modify Reason	Page	Note
MB1	Change R52 from @1.5M-04 to @1.5M-1-04	Change path to SB for ICH9M control CLK_PWGD timing change	7	
	Change C1408 from .1U-16-04Y-Z to @.1U-10-04X-K			
	Change R1363 from .@0-04 to 0-04			
MB2	Change power plane from +5VA to +5VS	Solve power LED double flash issue when Press power button to power on	19	
MB3	Del NB_R,NB_G,NB_B net name	Net error	15	
MB4	Correct power plane from +3VS to +3V	Follow Intel schematic	17	
MB5	L7 correct footprint to DFDH2012T package	Footprint error	20	
MB6	Add R1397 and change L35 to F50IN5 only	For M1 request	22	
	Del JP26,JP15		31	
MB7	Change U9 to F50IN5 only	For 8102E feature	22	
MB8	Change C1348,C1357 from 3300P-50-06X-K to 3300P-50-04X-K	Bom error	27	
MB9	Change C1405 from 22N-16-04X-K to .022U-50V-04Y-Z	Bom error	31	
MB10	Change R1315.R1316,R1317,R1318,R1324,R1325,R1326,R1327	For F50IN0 function	32	
	Add RN17,RN18,RN19,RN20			
	Add R1400		34	
	Add R1401		40	
MB11	Change R1301 from 0-04 to @0-04 and R1302 from @10K-04 to 10K-04	Disable LVDS B channel power supply	39	
MB12	Change R124,R125 from 2.2K-06 to @2.2K-06 and for F50IN5 only	For F50IN5 Hybrid function	9	
	Change Q128,Q129,R1388,R1389 for F50IN5 only			
	Change +5V to +5VA		32	
	Change U33,U35,U53,U54,U57,Q128,Q129,R1388,R1389,R1328,C1401,C860,C1399,R1314, C1407,R1343 for F50IN5 only			
	Change U33 footprint			
	Change Q84,Q85,C1361,C869,R850,C865,R848,C867 for F50IN5 only		33	
	Change U52,R1361,R1362,C1397 for F50IN5 only		34	
	Change +3VA to +3V		44	
	Change Q136 for F50IN5 only		40	
	Del U35 and C862		31	
MB13	Change R1307,R1308,R1309,R1310 for F50IN0 only	For F50IN0/IN5 disable NB CRT	9	
	Change R1309,R1310 from @0-04 to 0-04			
	Change R121,R122,R123 to option table			
	Change R207,R111,R112 for F50II0/IN5			
	Change C148,C158,C197,C210 to option table		11	
	Change B6,R169,C147,C159,R1311,R174 for F50II0 only			
MB14	Change swap SATA port 1 and port4	Solve ODD can't enable AHCI for new bios code	16	
	Change C365,C366 from 0-04 to .01U-16-04X-K			
	Change C493,C496 from .01U-16-04X-K to 0-04		20	
MB15	Change RN1 from 56-8P4R-04 to 56-8P4R-04-1	Bom eror	17	
	Change RN5,RN6,RN8,RN9,RN10,RN11,RN12,RN13,RN14,RN15,RN16 from 56-8P4R-04 to 56-8P4R-04-1		26	
MB16	Colayout with CH7318B	For CH7318A update IC version to CH7318B	14	
	Add R1402			
	Change R208 from 100K-04 to @100K-04			
	Change Q6 from FET-2N7002 to @FET-2N7002			
	Change R191 from @4.7K-04 to 4.7K-04			
	Change R194,R195,R199 from 10K-04 to @10K-04			
MB17	Change Q64 from @FET-P2003BVG to FET-P2003BVG	For S3 leakage current and power sequence	30	
MB18	Change CN24 pin define	For M2 and ME request	25	
MB19	Change R1198,R1199 from 4.7K-04 to 3.6K-04	Follow Realtek FAE comments	22	
	Change R1199 from @4.7K-04 to @3.6K-04			
MB20	Change R1329 from 0-04 to .1U-16-04Y-Z	For sourcer request	25	
	Change C1402 from @1U-10-04Y-Z to 1U-10-04Y-Z			
MB21	Change R1092,R1103 from 150K-1-04 to 0-04	Improve power off leakage current	28	
	Change C1209,C1214 from .01U-16-04X-K to 10P-25-04N			
MB22	Change R1062 from 11.5K-1-04 to 5.36K-1-04	Correct NVVDD OCP	45	
	Change R1058 from @100K-1-04 to 75K-1-04			
MB23	Change USW1 from @MLX90248 to @BU52026G	For sourcer request	48	
MB24	Change CN15 from CON-USB-1909574-1 to CON-USB-1759582-1	For EMI request	20	
	Change C1421 from @.1U-16-04Y-Z to 100P-50-04N-J		24	
	Change C1379,C1381,C1382 from @100P-50-04X-K to 100P-50-04N-J			
	Change C1414 from 10P-25-04N to 100P-50-04N-J and add C1437		33	
	Add C1431,C1433		30	
	Add C1432,C1434,C1435		29	
	Change C88,C89,C91,C95,C96 from @10P-25-04N to 100P-50-04N-J		7	
	Change C1246 from @.1U-25V-04Y-Z to 100P-50-04N-J		30	
	Add C1436 for all project		45	
	Change B58 from @BD-QT4532KL080HC to BD-QT4532KL080HC and add B107 ; del JP4		28	
	Change L2,L4 from @CK-ATCM2012-900T to CK-ATCM2012-900T		19	
	Del R370,R371,R383,R386			
	Change L8 from @CK-ATCM2012-900T to CK-ATCM2012-900T		27	
	Del R436,R437			
	Change C1393,C1379 net		24	
	Change C1379 from 100P-50-04N-J to @100P-50-04N-J			
	Change B59 type from BD-4516KF-600T60 to BD-QT2012KL120HC-5 and add B108 ; del JP7		29	
	Del B82		27	
	Change B94 type from BD-4516KF-600T60 to BD-HCB2012KF-800T50		45	
	Change B62 type from BD-4532KF-800T80 to BD-QT2012KL120HC-5 and add B109		31	
	Add C1438,C1439			
	Add C1440		13	
	Add C1441,C1442		20	
MB25	Change C735,C1403,C755 from 4.7U-10-08Y-Z to @4.7U-10-08Y-Z	Improve 3/5V power quality	28	
	Change C1219 from 470P-50-06N-K to 6.8N-16-04X-K			
	Add C1430			
	Del C1403			
MB26	Add H24,H25	Improve PCB strength on NB and GPU	31	
	Change H22,H23 footprint from holetc197bc79d79i99 to HOLEC79D79N to be NPTH HOLE	For ME request		
MB27	Change R1178 from 1K-04 to @1K-04	Change Lan power path	22	
	Change R1166 from @0-06 to 0-06			
	Change R1171 from 100K-04 to @100K-04			
	Change Q108 from FET-SI2301BDS to @FET-SI2301BDS			
	Change Q109 from FET-2N7002 to @FET-2N7002			
MB28	Add D57,D58	Reserved ESD solution for USB port	20	
	Add UD1,UD2,UD3,UD4		48	
MB29	Change C1342 from .1U-16-04Y-Z to 4.7U-6.3-06R	For new Card +1.5V_PCIE drop issue	21	
	Change C552 from .1U-16-04Y-Z to 1U-10-04Y-Z			
MB30	Add R1403	Add VL current sink path	28	
MB31	Change CN7 DMic pin define	For ME request	19	
MB32	Change Q137,R1390,R1275,R1350,R1351,R1352,R1353,R1274 for F50IN5 only	For F50IN5 Hybrid	17	
MB33	Change R1370,R1371from 0-04 to @0-04	Option for CRT EDID	32	
MB34	Add R1404,R1405,R1406,R1407,R1408	Colayout Mini PCI 1.1/1.2 power plane	21	
MB35	Change power plane from VDD33 to +5V_GPU	Solve HDMI noise when HP Jack plug in	40	
MB36	Change C1042 footprint from M-C0603 to M-C0402	Footprint error	39	
MB37	Change L16 for F50II0 only	For CRT ripple issue	28	
	Add L36			
MB38	Change R255 from 22.6-1-04 to 19.6-1-04	Improve SATA signal quality	16	
MB39	Change H18 footprint	For M1 request	31	
	Change JP22 footprint		26	
	Change RAD1 package			
	Change RCH1 package			
	Del R709 and add JP26		29	
	Change CN27 footprint		44	
MB40	Change C1219 footprint from M-C0603 to M-C0402	Footprint error	28	
MB41	Change R1041 from 0-06 to BD-QT1608BL300	For EMI request	44	
	Change B67,B68,B69 from BD-QT1608RL060 to BD-QT1608RL030HC			
	Change R1297,R1298 from BD-QT1005RL030 to BD-QT1608BL040		15	
	Change B29,B30,B31 from BD-QT1608RL060 to BD-QT1608RL030HC			
	Change L11 from CK-223LC0801T2.2 to CK-ARI223LC0801TA		23	
	Change L33,L34 from CK-223LC0801T2.2 to CK-ARI223LC0801TA		22	
	Add R1409,R1410		19	
	Change C1379 from @100P-50-04N-J to 100P-50-04N-J		24	
	Add C1443,C1444			
MB42	Change L34 for F50IN5 only	For F50IN5 only	22	
MB43	Change R1112 to option table	For different choke type change OCP setting	28	
MB44	Change R205 table for F50IN0/IN5	Table error	6	
MB45	Change R207 for F50II0 only	For F50II0 only	6	
MB46	Change R1307,R1308,R1309,R1310 for F50IN0/IN5	For F50IN0/IN5 disable NB CRT	9	
MB47	Change C147 from .1U-16-04Y-Z to .01U-16-04X-K	For Bom control easy	11	
	Change C148 from .01U-16-04X-K to .1U-16-04Y-Z			
MB48	Change C1303 and R1195,R1198,R1199 for F50IN5 only	For 8111C only	22	
MB49	Change R1156 from @1K-04 to 1K-04	For +3.3VA current sink path	30	
	Change C1260 from @.1U-16-04Y-Z to .1U-16-04Y-Z			
	Change R519 from @0-04 to 0-04			
MB50	Change C655 from @.1U-16-04Y-Z to @.1U-25-06Y-Z	Footprint error	25	
MB51	Change R1207,R942 from 10K-04 to 2.2K-04	For NV request to improve HDCP CLK/DAT rise time	40	
MB52	Change R937 for F50IN5 only and change value from @3.4K-1-04 to 36K-1-04	For NV request to solve HDMI Audio pop noise for NB9P	40	
MB53	Change C1052 to option table	For NV request to solve HDMI Audio pop noise for NB9P/M	40	
MB54	Change C1402 from 1U-10-04Y-Z to @1U-10-04Y-Z and update option table	To fix ITE8512-JX 3.3V leakage current	25	

F50 RC to F71 RC Modify list:

Symbol	Modify Item	Modify Reason	Page	Note
MC1	Stuff R1301, replace R1302	F71Ixx use LVDS dual channel	39	
MC2	Stuff RN19,RN20	F71Ixx use LVDS dual channel	32	

Title	F71IXX		
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	Del B82		27	
	Change B94 type from BD-4516KF-600T60 to BD-HCB2012KF-800T50		45	
	Change B62 type from BD-4532KF-800T80 to BD-QT2012KL120HC-5 and add B109 Add C1438,C1439		31	
	Add C1440		13	
	Add C1441,C1442		20	
MB25	Change C735,C1403,C755 from 4.7U-10-08Y-Z to @4.7U-10-08Y-Z Change C1219 from 470P-50-06N-K to 6.8N-16-04X-K Add C1430 Del C1403	Improve 3/5V power quality	28	
MB26	Add H24,H25 Change H22,H23 footprint from holetc197bc79d79i99 to HOLEC79D79N to be NPTH HOLE	Improve PCB strength on NB and GPU For ME request	31	
MB27	Change R1178 from 1K-04 to @1K-04 Change R1166 from @0-06 to 0-06 Change R1171 from 100K-04 to @100K-04 Change Q108 from FET-SI2301BDS to @FET-SI2301BDS Change Q109 from FET-2N7002 to @FET-2N7002	Change Lan power path	22	
MB28	Add D57,D58	Reserved ESD solution for USB port	20	
	Add UD1,UD2,UD3,UD4		48	
MB29	Change C1342 from .1U-16-04Y-Z to 4.7U-6.3-06R Change C552 from .1U-16-04Y-Z to 1U-10-04Y-Z	For new Card +1.5V_PCIE drop issue	21	
MB30	Add R1403	Add VL current sink path	28	
MB31	Change CN7 DMic pin define	For ME request	19	
MB32	Change Q137,R1390,R1275,R1350,R1351,R1352,R1353,R1274 for F50IN5 only	For F50IN5 Hybrid	17	
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MB49	Change R1156 from @1K-04 to 1K-04 Change C1260 from @.1U-16-04Y-Z to .1U-16-04Y-Z Change R519 from @0-04 to 0-04	For +3.3VA current sink path	30	
MB50	Change C655 from @.1U-16-04Y-Z to @.1U-25-06Y-Z	Footprint error	25	
MB51	Change R1207,R942 from 10K-04 to 2.2K-04	For NV request to improve HDCP CLK/DAT rise time	40	
MB52	Change R937 for F50IN5 only and change value from @3.4K-1-04 to 36K-1-04	For NV request to solve HDMI Audio pop noise for NB9P	40	
MB53	Change C1052 to option table	For NV request to solve HDMI Audio pop noise for NB9P/M	40	
MB54	Change C1402 from 1U-10-04Y-Z to @1U-10-04Y-Z and update option table	To fix ITE8512-JX 3.3V leakage current	25	