

6. Circuit Descriptions

6-1 S.M.P.S.

6-1-1 Comparison between Linear Power Supply and S.M.P.S.

6-1-1 (a) Linear

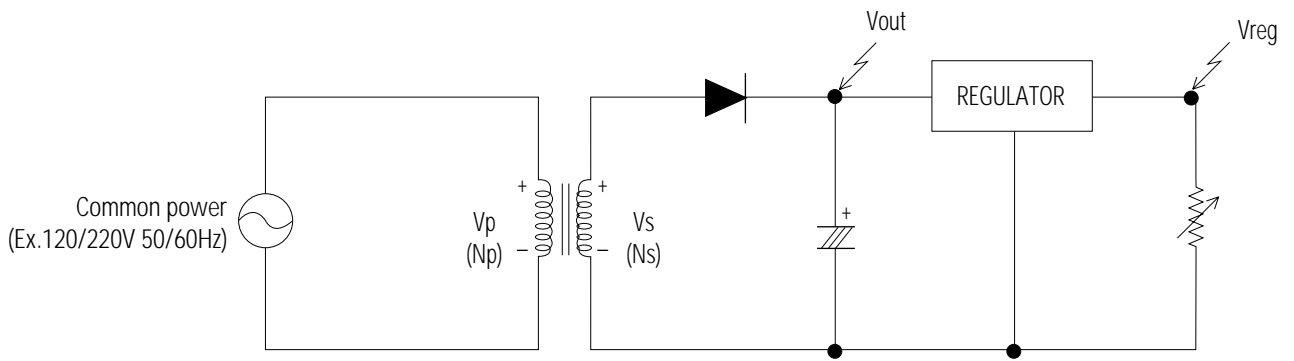


Fig. 6-1 Linear Power Supply

◆ Waveform/Description

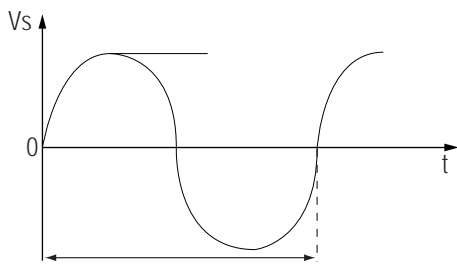


Fig. 6-2

Input : Common power to transformer (V_p).

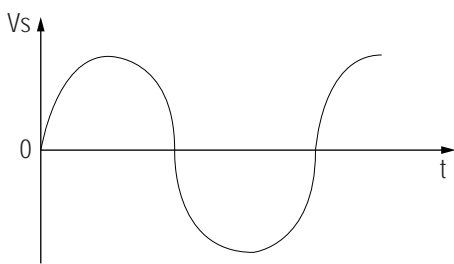


Fig. 6-3

The output V_s of transformer is determined by the ratio of 1st N_p and 2nd N_s .
 $V_s = (N_s / N_p) \times V_p$

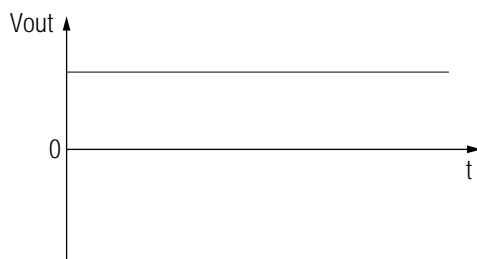


Fig. 6-4

V_{out} is output (DC) by diode and condenser.

◆ Advantages and disadvantages of linear power supply

1) Advantages : Little noise because the output waveform of transformer is sine wave.

2) Disadvantages :

- ❶ Additional margin is required because V_s is changed (depending on power source). (The regulator loss is caused by margin design).
- ❷ Greater core size and condenser capacity are needed, because the transformer works on a single power frequency.

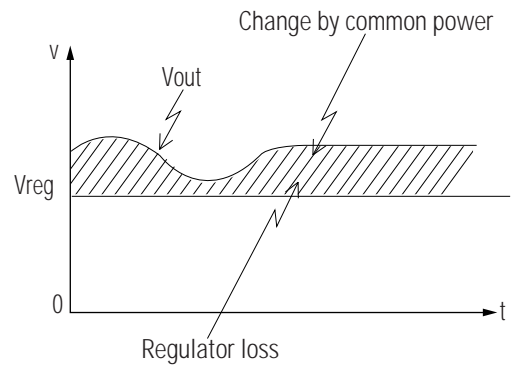


Fig. 6-5

6-1-1 (b) S.M.P.S. (Pulse width modulation method)

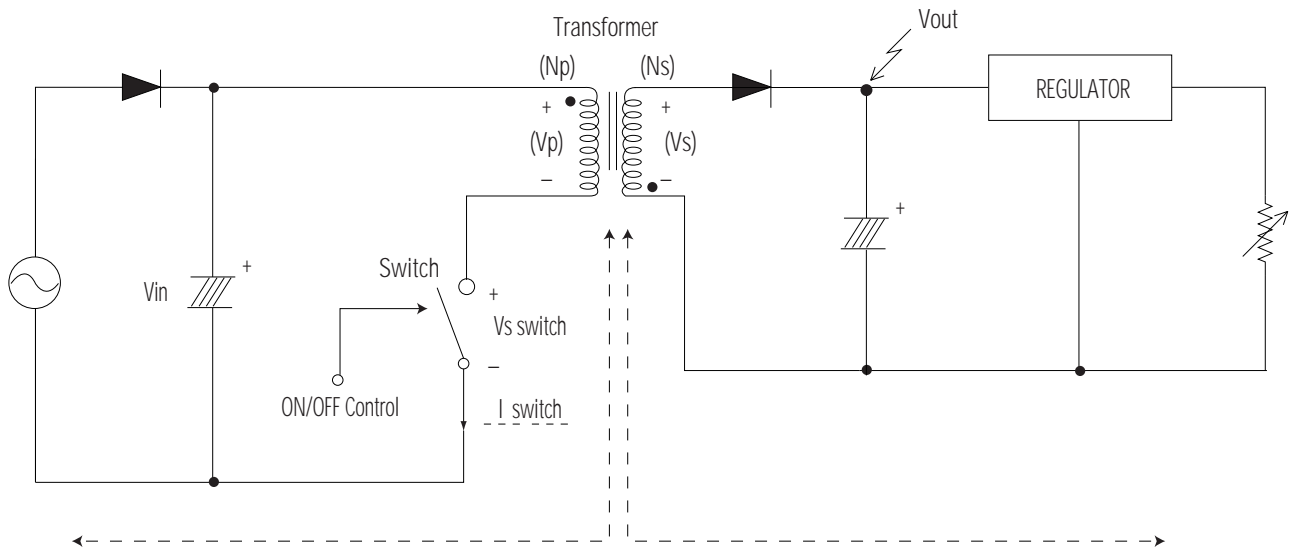


Fig. 6-6

◆ Terms

- 1) 1st : Common power input to 1st winding.
- 2) 2nd : Circuit following output winding of transformer.
- 3) f (Frequency) : Switching frequency (T : Switching cycle)
- 4) Duty : $(T_{on}/T) \times 100$

6-1-2 Circuit description (FLY-Back PWM (Plise Width Modulation) Control)

6-1-2 (a) AC Power Rectification/Smoothing Terminal

- 1) PD01,PD02,PD03,PD04 : Convert AC power to DC(Wave rectification)
- 2) PE3 : Smooth the voltage converted to DC(Refer to VIN of Fig. 6-7)
- 3) PC01, PC02, PC10, PC11, PC12, PC13, PL01, PL02, PL03 : Noise removal at power input/output
- 4) PVA1 : SMPS protection at power surge input (PVA1 pattern open is to remove noise)
- 5) PR10 : Rush current limit resistance at the moment of power cord insertion.
 - ❶ Rush current = (AC input voltage x 1.414 - Diode drop voltage) / Pattern resistance + PL02,01 resistance + PC10 resistance + PR10) (AC230V based : approx. 26A)
 - ❷ Without PR10, the bridge diode might be damaged as the rush current increases.

6-1-2 (b) SNUBBER Circuit : PR15, PR16, PC04, PC05, PD11, PR17

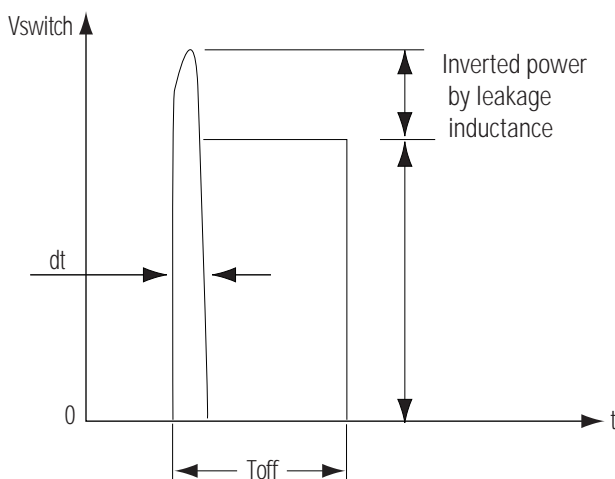


Fig. 6-7

- 1) Prevent residual high voltage at the terminals of switch during switch off/Suppress noise. High inverted power occurs at switch (PIC1) off, because of the 1st winding of transformer : ($V = LI \times di/dt$. LI : Leakage Induction) A very high residual voltage exists on both terminals of PIC1 because dt is a very short.
- 2) SNUBBER circuit protects PIC1 from damage through leakage voltage suppression by RC, (Charges the leakage voltage to PD11 and PC04, and discharges to PR15 and PR16).
- 3) PC05, PR17 : For noise removal

6-1-2 (c) PIC1 Vcc circuit

- 1) PR11, PR12, PR13, PR14 : PIC1 driving resistance (PIC1 works through driving resistance at power cord in)
- 2) PIC1 Vcc : PR18, PD12, PE6
 - ❶ Use the output of transformer as Vcc, because the current starts to flow into transformer while PIC1 is active.
 - ❷ Rectify to PD12 and smooth to PE6.
 - ❸ Use the output of transformer as PIC1 Vcc : The loads are different before and after PIC1 driving. (Vcc of PIC1 decreases below OFF voltage, using only the resistance due to load increase after PIC1 driving.)

6-1-2 (d) Feedback Control Circuit

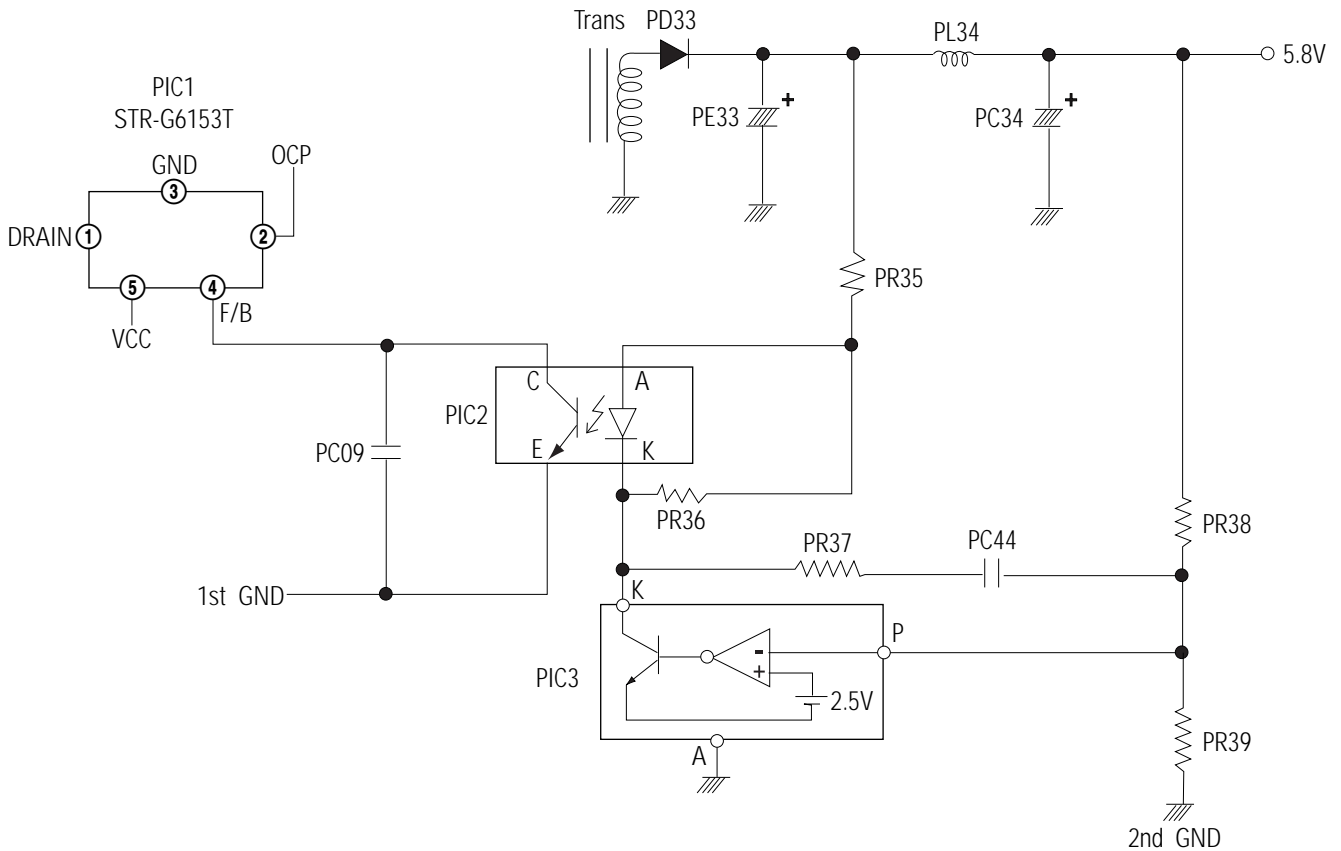


Fig. 6-8

- 1) F/B terminal of PIC1 determines output duty cycle.
- 2) C-E(Collector-Emitter) of PIC2 and F/B potential of PIC1 are same.

◆ Operation descriptions

- 1) Internal OP-Amp '+' base potential of PIC3 is 2.5V and external '-' input potential is connected with PR38 and PR39 to maintain V_{out} of 5.8V. ($V_{out} = ((PR36 \times PR39) / PR39) \times 2.5V$)
- 2) If load of 5.8 V terminal increases(or AC input voltage decreases) and V_{out} decreases below 5.8V, then :
 PIC3 'P' potential down below 2.5V --> PIC3 A-K of base current down --> PIC3 of A-K current down -->
 PIC2 Diode current down --> PIC2 C-E current down --> PIC2 C-E voltage up --> PIC1 F/B voltage up -->
 Out Duty up --> Transformer 1st current up --> Transformer 1st power up --> V_{out} up --> Maintain V_{out} 5.8V
- 3) If load of 5.8 V terminal decreases(or AC input voltage rises) and V_{out} rises above 5.8V, then :
 Reverse sequence of the above description --> Duty down --> V_{out} down --> Maintain 5.8V (i.e., the feedback to maintains 5.8V).
 - ❶ PR35, PR36 : Reduce 5.8V overshoot
 - ❷ PR37, PC44 : Prevent PIC3 oscillation(for phase correction)
 - ❸ PC09 : Adjust feedback response rate

6-1-3 Internal Block Diagram

6-1-3 (a) Internal Block Diagram of S.M.P.S. Circuit

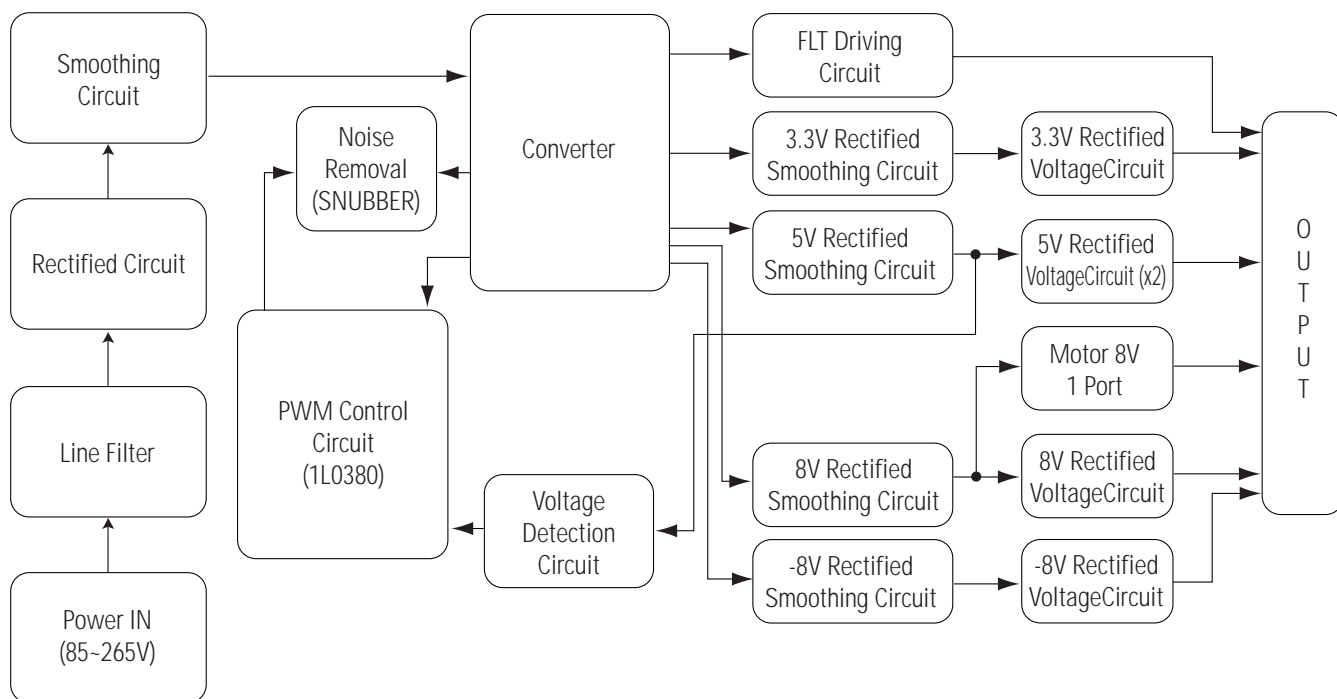


Fig. 6-9

6-1-3 (b) PIC1 (STR-G6153T) Internal Block Diagram

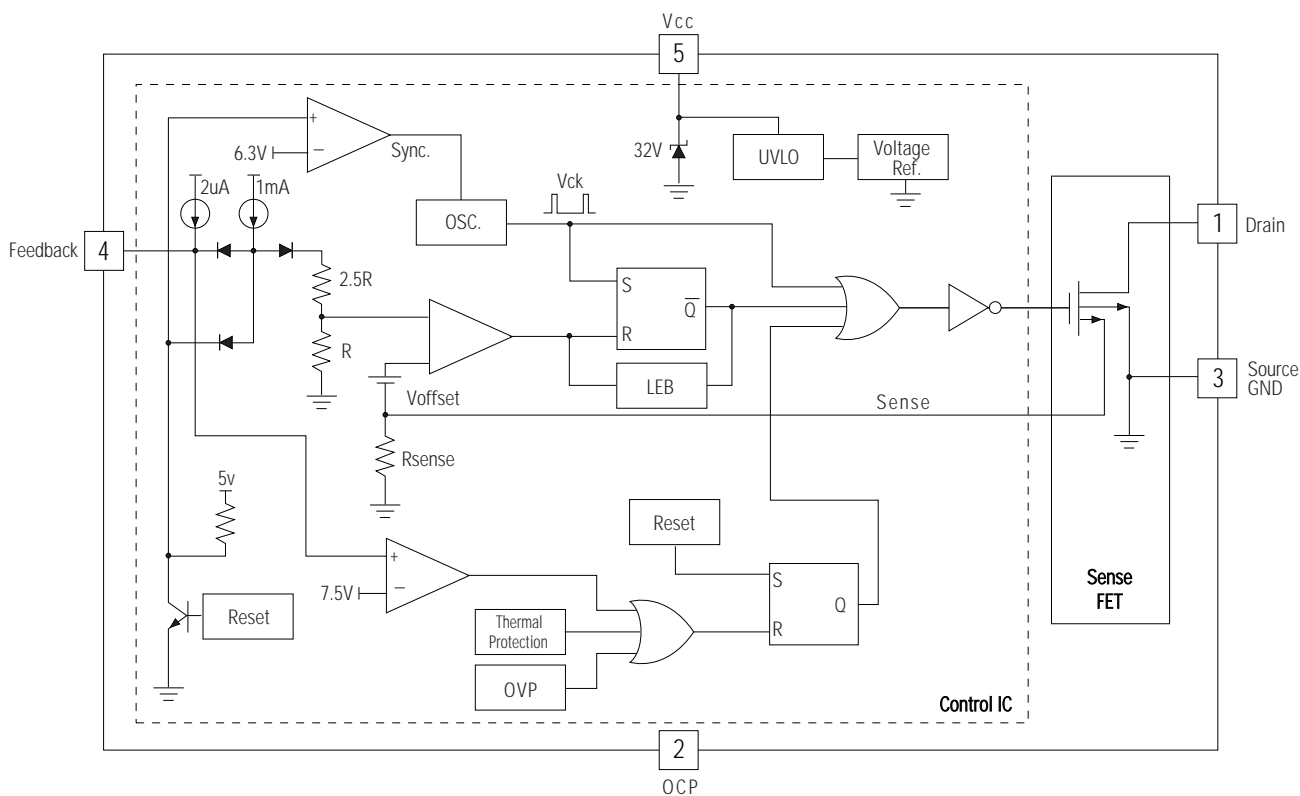


Fig. 6-10

6-2 RF

6-2-1 RIC1 (KS1461)

KS1461 is combined with KS1452 and KS1453 as bipolar IC developed for DVD SERVO system. Main features include DVD waveform equalizing, CD waveform equalizing, focus error signal generation, 3-beam tracking error signal generation, DPD 1-beam tracking error, defect, envelope, MIRR output, etc. after receiving the pick-up output converted into I/V.

6-2-1 (a) Basic Potentiometer

KS1461 uses a single power method and each circuit is based on V of 2.5V. V (Pin 12, 20, 24, 67) terminal is needed for IC, which uses the peripheral V.

6-2-1(b) RF signal

Fig. 6-11 shows the flow of signal generated by the pick-up. A, B, C, D signals detected from pick-up are converted in to RF signal(A+B+C+D) via RF summing AMP.

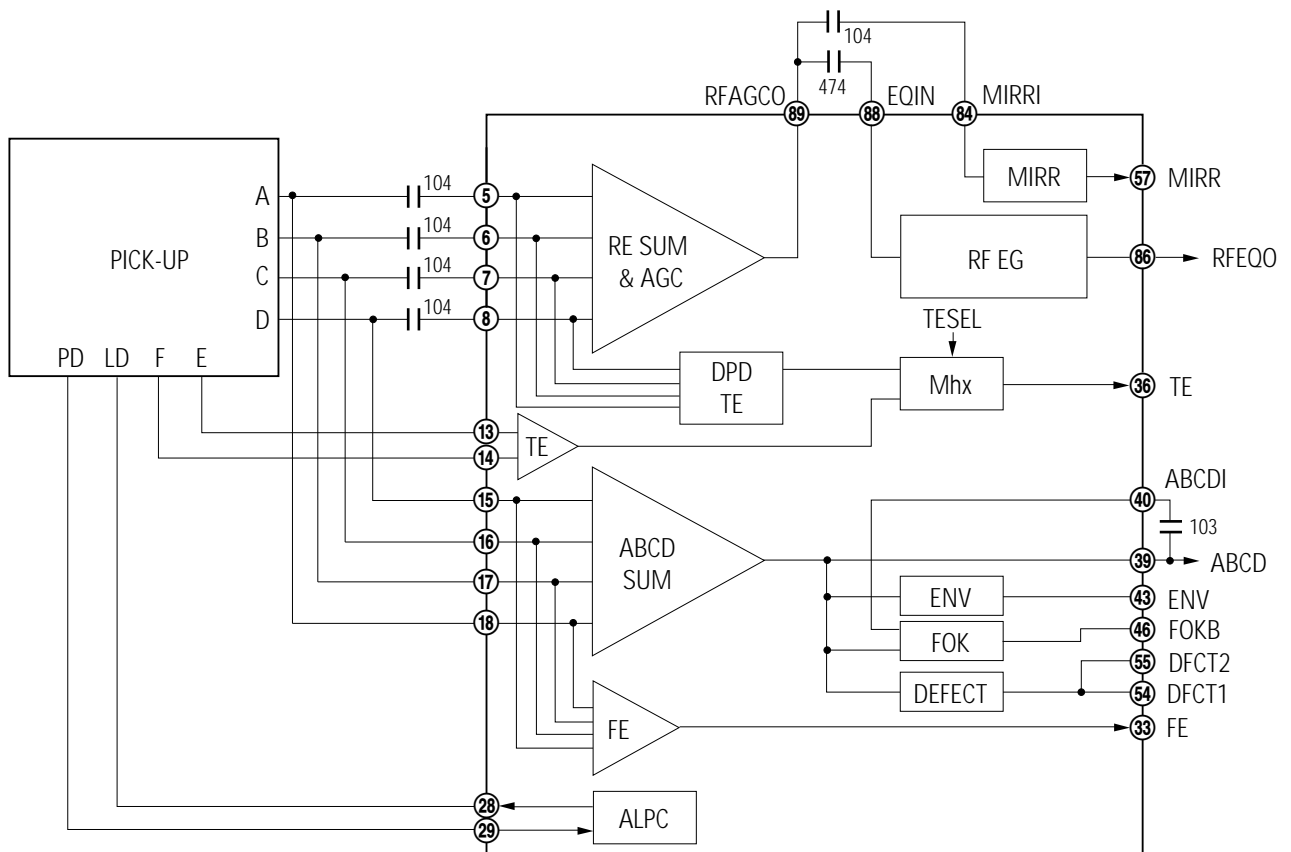


Fig. 6-11

Fig. 6-12 shows the waveform-equalizing block diagram for the RF signal. It outputs to EQout (Pin 86) terminal by initially changing switching AMP gain of DVD and CD, and then adjusting the level in RF SUM & AGC. It controls RF SUM & AGC gain by means of Pin 89-95 and interfaces with PWM signal, (output from PWM terminal of KS1453, via low-pass filter to adjust boost gain and peak frequency. EQout terminal is connected with EQin (Pin 86).

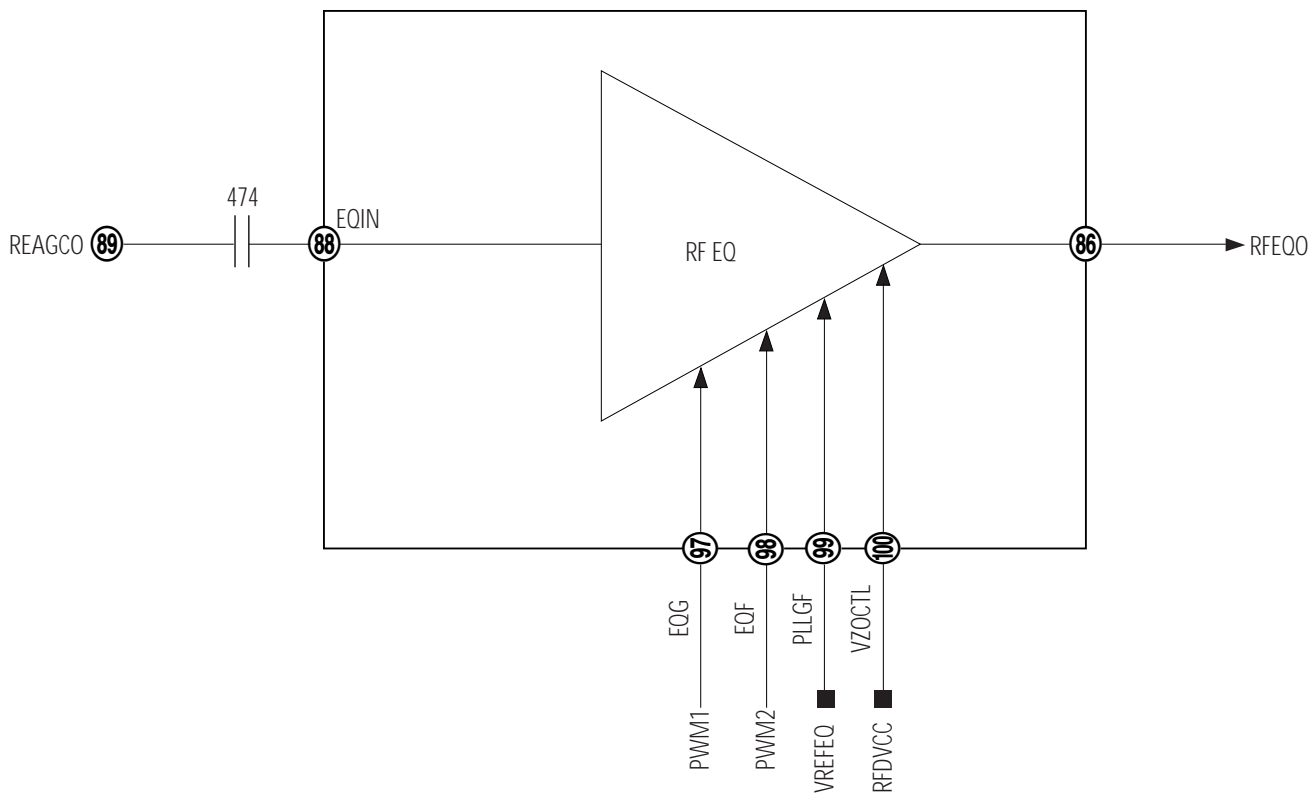


Fig. 6-12

The control parameters of DVD EQ and CD EQ are as follows.

1) DVD CD EQ control parameter

- ❶ EQG (Pin 97) : Changes the gain of peak frequency with EQ frequency characteristic. Convert PWM signal, output from KS1453, into DC via low-pass filter.
- ❷ EQF (Pin 98) : Changes the peak frequency with EQ frequency characteristic. Convert PWM signal, output from KS1453, into DVD via low-pass filter.

6-3 System Control

6-3-1 Outline

The main micom peripheral circuit is composed of 16bit Micom (MIC1 ; TMP93CM41F), 8M EPROM (MIC8 ; AM27C080) for Microcode and data save, 512 byte EE-PROM (MIC5 ; KS24C020) for permanent storage of data needed at power off, MIC4 (74AC573) to latch only address in the bus where address and data are mixed, address decoder (MIC7 ; 74HC00) for selection of external device chip and 20MHz clock oscillator for micom operation. The Micom (MIC1 ; TMP93CM41F) mounted in main board analyzes the key commands of front panel or instructions of remote control through communication with Micom (FIC1 ; LC86P6232) of front and controls the devices on board to execute the corresponding commands after initializing the devices connected with micom on board at power on.

6-3-2 Block Diagram

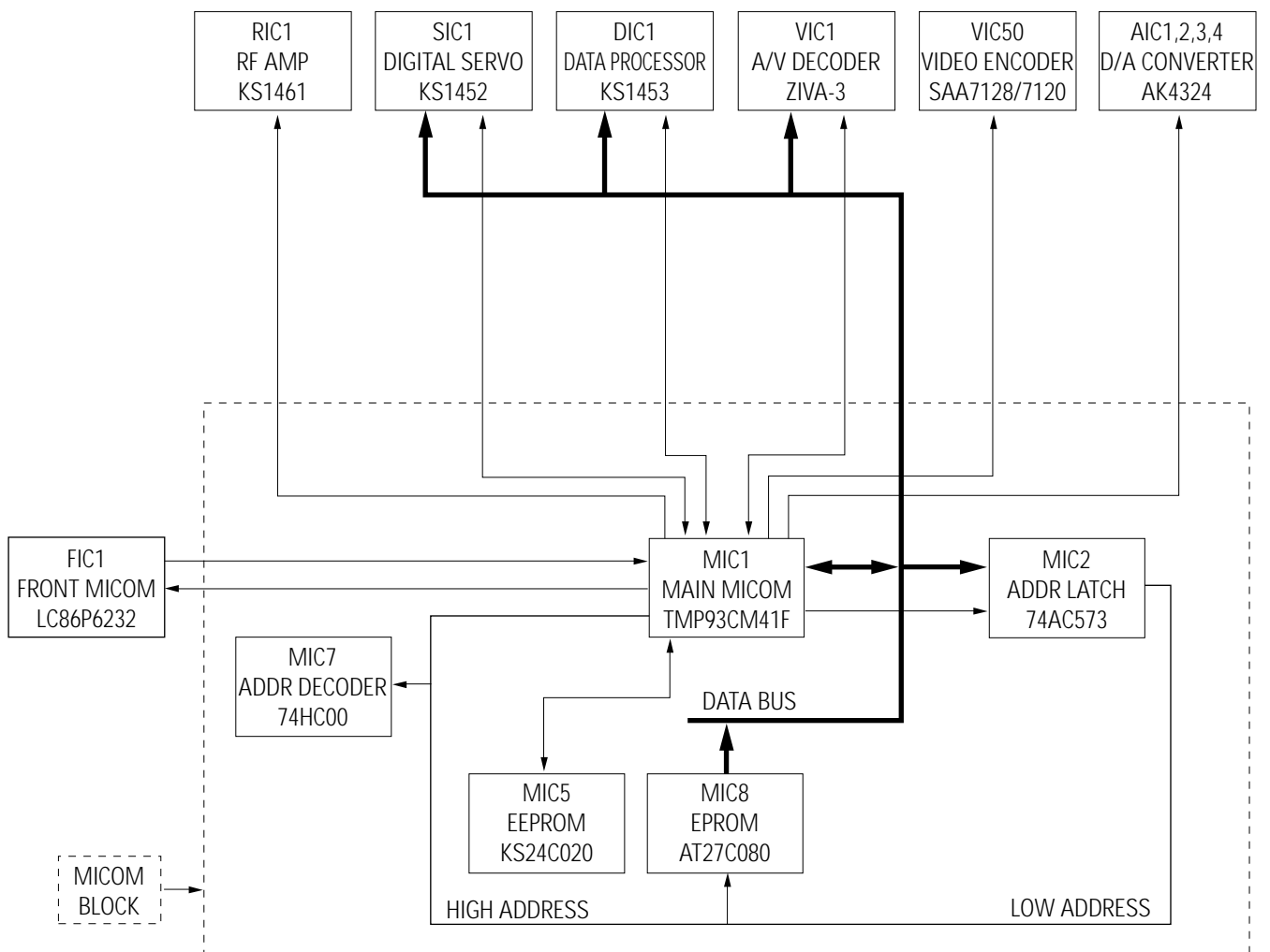


Fig. 6-13

6-3-3 Waveform Description

When micom accesses each device sharing bus, it falls the chip select signal of corresponding chip to (CS2:MIC8-22, /DSPCS:DIC1-2, /DVDCS:VIC1-206/SRVCS:SIC1-10) 0 (Low) before trial.

So to speak, the bus is used by time-division as shown in Fig 6-14, 6-15, 6-16.

Two and more devices can't be accessed simultaneously.

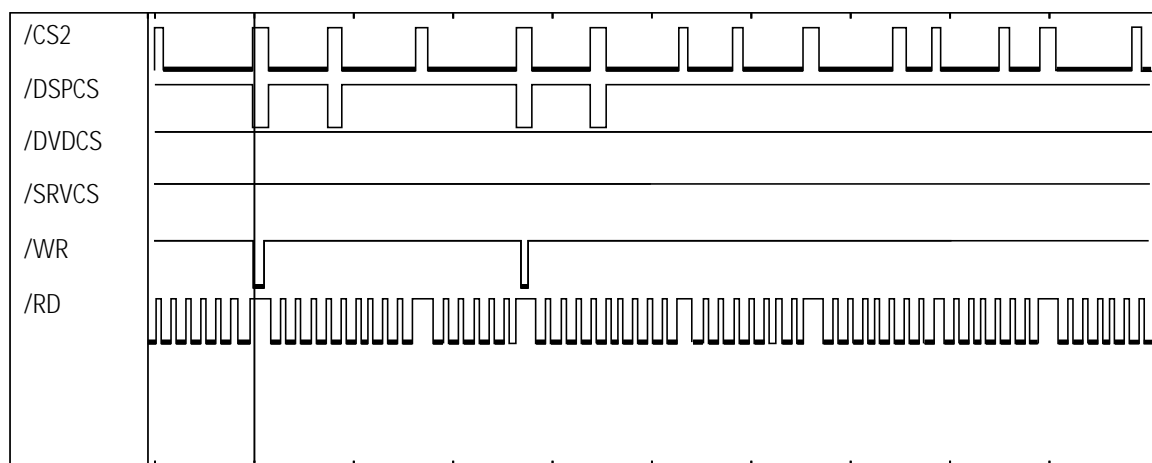


Fig. 6-14

- CH1 : CS2 (MIC8-22, EPROM CHIP SELECT)
- CH2 : DSPCS (DIC1-2, DATA PROCESSOR CHIP SELECT)
- CH3 : DVDCS (VIC1-206, A/V DECODER CHIP SELECT)
- CH4 : SRVCS (SIC1-10, DIGITAL SERVO CHIP SELECT)
- CH5 : WR (MIC1-73, MICOM OUTPUT WRITE SIGNAL)
- CH6 : RD (MIC1-72, MICOM OUTPUT READ SIGNAL)

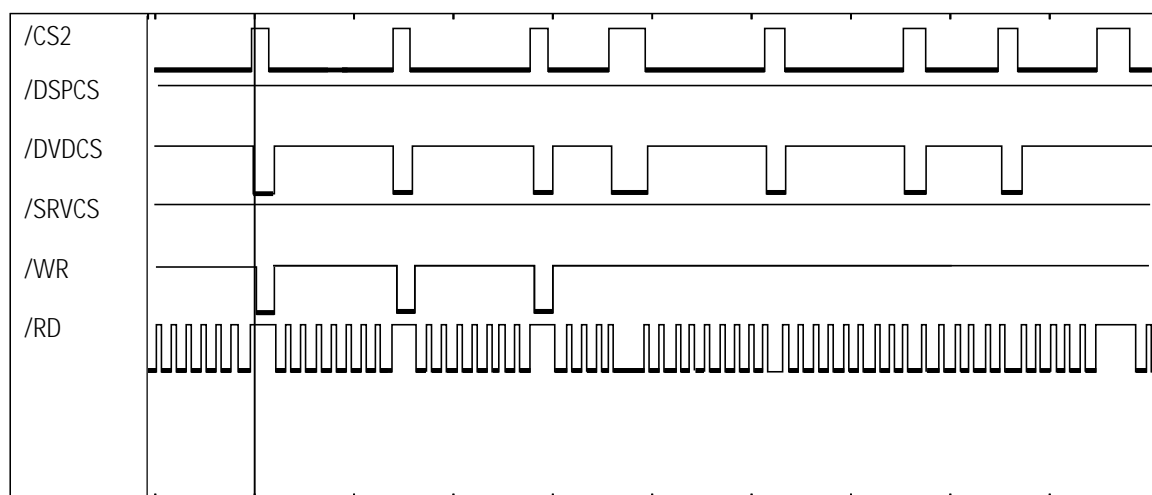


Fig. 6-15

- CH1 : CS2 (MIC8-22, EPROM CHIP SELECT)
- CH2 : DSPCS (DIC1-2, DATA PROCESSOR CHIP SELECT)
- CH3 : DVDCS (VIC1-206, A/V DECODER CHIP SELECT)
- CH4 : SRVCS (SIC1-10, DIGITAL SERVO CHIP SELECT)
- CH5 : WR (MIC1-73, MICOM OUTPUT WRITE SIGNAL)
- CH6 : RD (MIC1-72, MICOM OUTPUT READ SIGNAL)

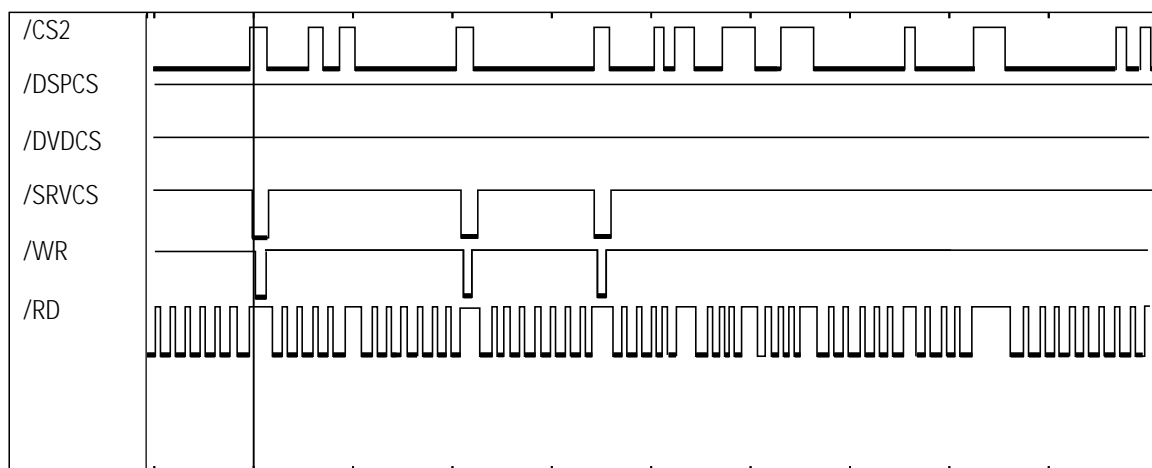


Fig. 6-16

- CH1 : CS2 (MIC8-22, EPROM CHIP SELECT)
- CH2 : DSPCS (DIC1-2, DATA PROCESSOR CHIP SELECT)
- CH3 : DVDCS (VIC1-206, A/V DECODER CHIP SELECT)
- CH4 : SRVCS (SIC1-10, DIGITAL SERVO CHIP SELECT)
- CH5 : WR (MIC1-73, MICOM OUTPUT WRITE SIGNAL)
- CH6 : RD (MIC1-72, MICOM OUTPUT READ SIGNAL)

6-4 Servo

6-4-1 Outline

SERVO system of DVD is divided into Focusing SERVO, Tracking SERVO, SLED Linked SERVO and CLV SERVO (DISC Motor Control SERVO).

1) Focusing SERVO

Focuses the optical spot output from object lens onto the disc surface. Maintains a uniform distance between object lens of Pick-up and disc (for surface vibration of disc).

2) Tracking SERVO

Make the object lens follow the disc track in use of tracking error signal (created from Pick-up).

3) SLED Linked SERVO

When the tracking actuator inclines outwardly as the object lens follows the track during play, the SLED motor moves slightly (and counteracts the incline).

4) CLV SERVO (DISC Motor Control SERVO)

Controls the disc motor to maintain a constant linear velocity (necessary for RF signal).

6-4-2 Block Diagram

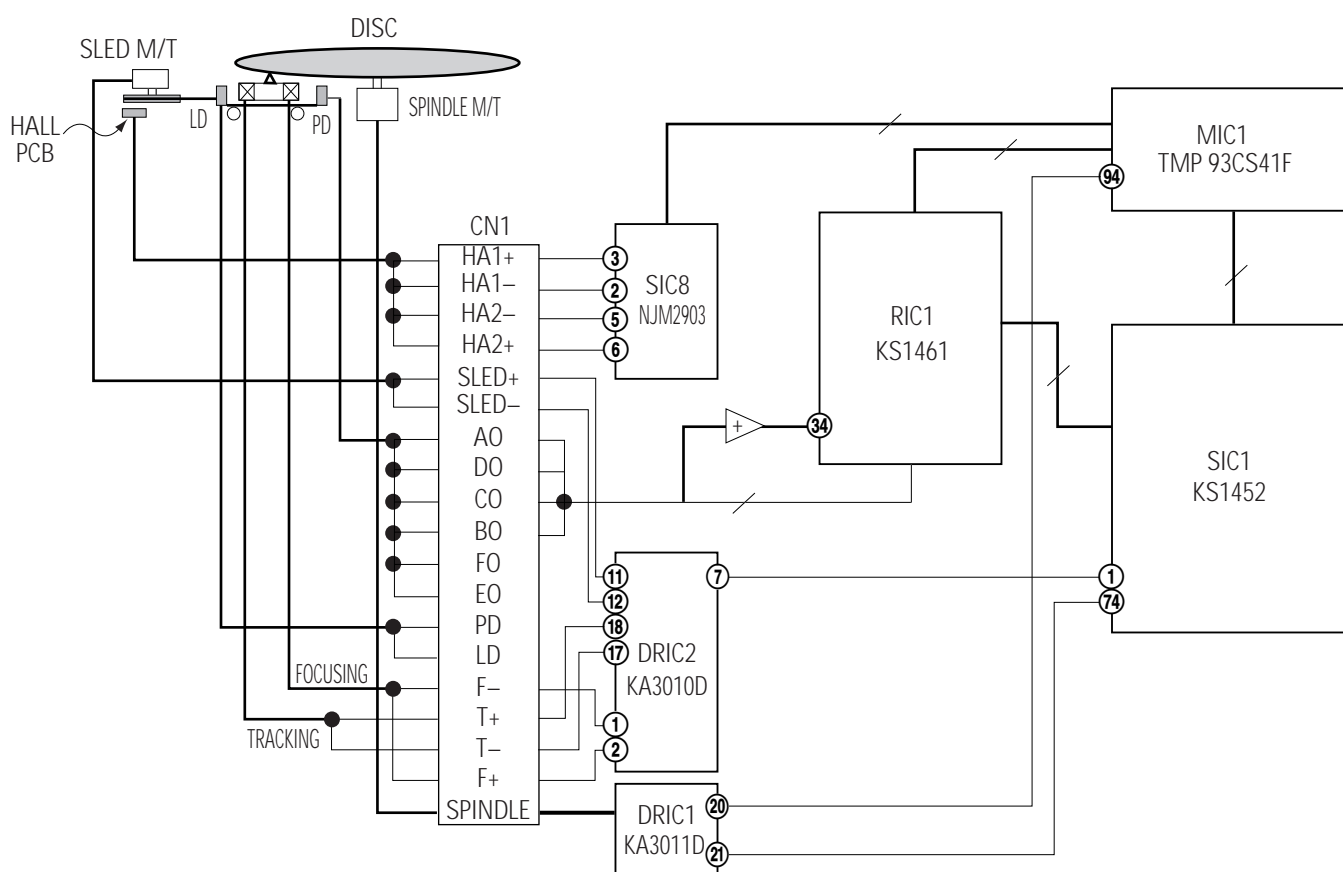


Fig. 6-17

6-4-3 Operation

1) FOCUSING SERVO

(1) FOCUS INPUT

The focus loop is changed from open loop to closed loop, and the triangular waveform moves the object lens up and down (at pin 75 of SIC1 during Focus SERVO ON.) At that time, S curve is input to pin 65 of SIC1.

ABAD (pin 39 of RIC1) signal, summing signal of PD A, B, C, D, is generated, and zero cross(2.5V) point occurs when S curve is focused and ABAD signal exceeds a preset, constant value. The focus loop is changed to closed loop, and the object lens follows the disc movement, maintaining a constant distance from the disc. (these operations are same in CD and DVD).

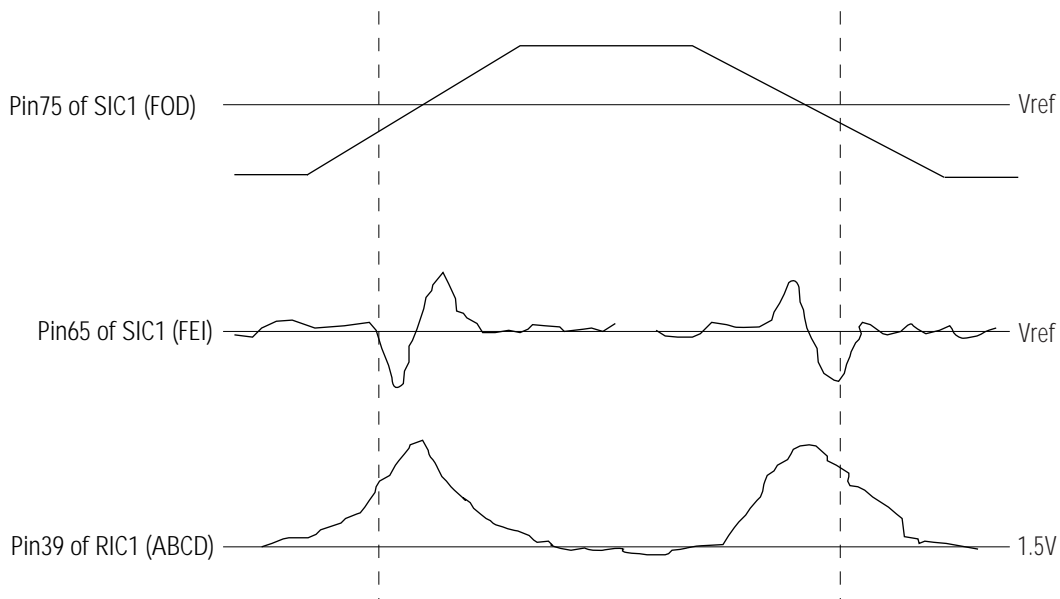


Fig. 6-18

(2) PLAY

When focus loop closes the loop during focus servo on, both pin 65 and pin 75 of SIC1 are controlled by VREF voltage (approx. 2.5V), and pin 1, 2 of DRIC2 are approximately 4.5V.

2) TRACKING SERVO

(1) NORMAL PLAY MODE

① For DVD

Composite : The signal output from PD A, B, C, D of Pick-up, the tracking error signal (pin36 of RIC1) uses the phase difference of A+C and B+D in RIC1, and inputs to terminal 64 of SIC1. Then, it is output to SIC1 pin 76 via digital equalizer, and applied to the tracking actuator through DRIC2.

Pins 17, 18 of SIC1 are controlled by VREF(approx. 2.5V) during normal play.

Meanwhile, DVD repeats the track jump from 1 to 4 in inner direction at normal play (because data- read speed from disc is faster than data output speed on screen).

② For CD, VCD

Receive the signal output through E, F of Pick-up, from RIC1. The tracking error signal is similar to DVD.

(2) SEARCH Mode :

Search mode : Fine seek,(Moving the tracking actuator slightly little below 255 track) and coarse search, moving much in use of sled motor. The coarse search will be described in sled linked servo and now, the fine seek is explained shortly.

If the object lens is located near target, cut off the tracking loop and give the control signal as many as desired count to move the tracking actuator via SIC1 pin 76 terminal(TRD).

3) SLED LINKED SERVO

- Normal play mode

Move SLED motor slightly by means of PWM signal in SIC1 pin 73, as the tracking actuator moves along with track during play. Control to move the entire Pick-up as the tracking actuator moves.

- Coarse search mode

In case of long-distance search (such as chapter search), SIC1 uses sled FG (SIC8 pin 1, 7, which is generated) by rotation of sled motor via hall PCB. Then, read ID and compute the existing track count after input of next track. If the existing track count is within fine seek range, tracking begins using fine seek.

4) CLV SERVO(DISC MOTOR CONTROL SERVO)

Input RF signal (from Pick-up) to SIC1 pin59. Detect SYNC signal from RF in SIC1, and output PWM signal to SIC1 pin 55 for constant linear velocity.

6-5 DVD Data Processor

6-5-1 Outline

DIC1(KS1453) performs Sync detection, EFM/EFM demodulation and error correction and Spindle motor control (CLV control) after inputting sliced EFM signal of RF signal at disc playback and EFM read clock (PLCK) signal generated from PLL. Outputs data which converted to the last audio and video from A/V decoder(VIC1). KS1453 uses external memory(4M DRAM) as buffer as well as for error correction and carries out Variable Bit Rate transfer function. VBR function uses the external buffer as buffer to absorb the difference of transfer rate occurring because the transfer rate of disc playback is faster than data transfer rate demanded by A/V decoder(Video/Audio Signal Process Chip).

In case of general disc refresh, the memory is almost filled up periodically. It is because Write rate to memory after disc playback and signal process is faster than Read of A/V decoder. When the memory is filled, this status is reported by interrupt to main micom, which controls the servo to kick back the pick-up to the previous track after memorizing the last data read from disc until now. It takes some times to jump to the previous track and return to the original(jump location) again. The memory will have an empty space because A/V decoder reads out data of memory.

When the memory has an empty space, where data can be processed and written and the pick-up correctly gets to the original location(before kick back location) again, it reads data again avoids the interrupt of data read previously. The basic operation repeats to perform as described above.

6-5-2 Block Diagram

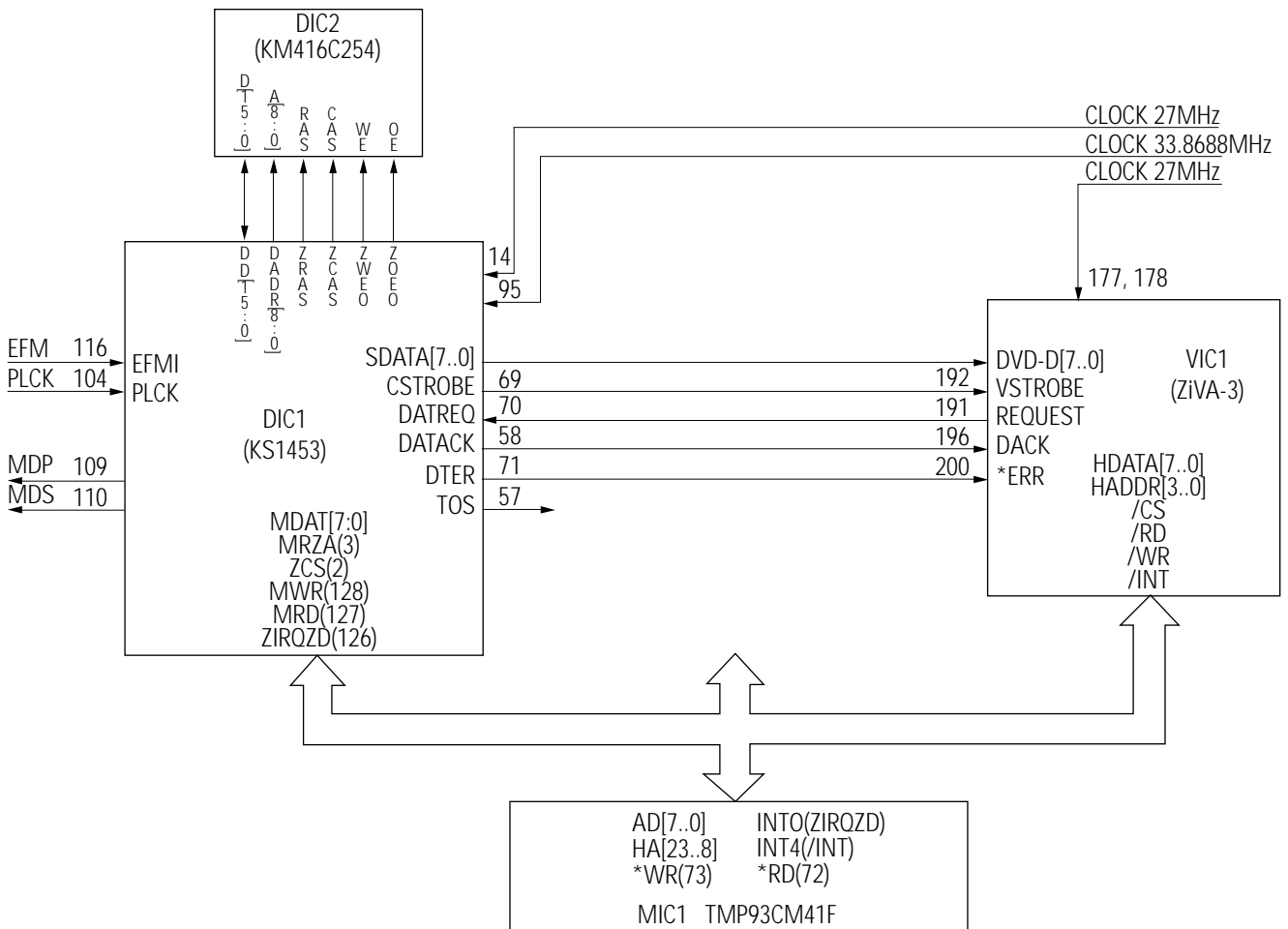


Fig. 6-19

6-5-3 Waveform Description

It measures the timing that data processed in DIC1 at DVD playback.

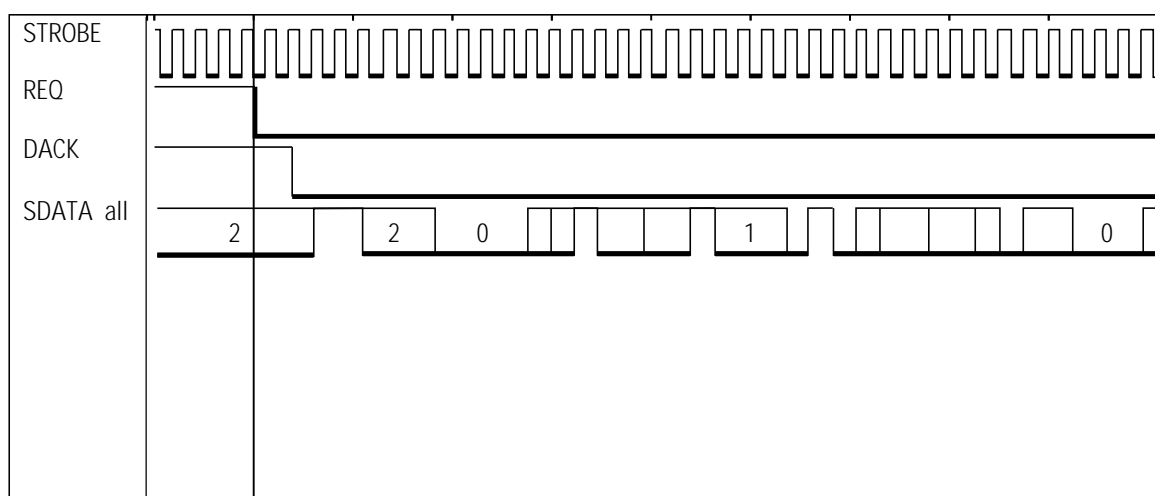


Fig. 6-20

- CH1 : STROBE (DIC1-69, CLOCK)
- CH2 : REQ (DIC1-70, DATA REQUEST)
- CH3 : DACK (DIC1-58, DATA ACKNOWLEDGE)
- CH4 : SDATA (DIC1-60-67, DATA)

6-6 Video

6-6-1 Outline

VIC50 sends VSYNC and HSYNC from VIC1(A/V decoder) and receives 8bit video data.

VIC50 does RGB encoding, copy guard processing and D/A conversion of 8bit video data inputted from VIC1(A/V decoder) by control of MIC1(Micom).

Video signal converted into analog signal is outputted via amplifier of analog part.

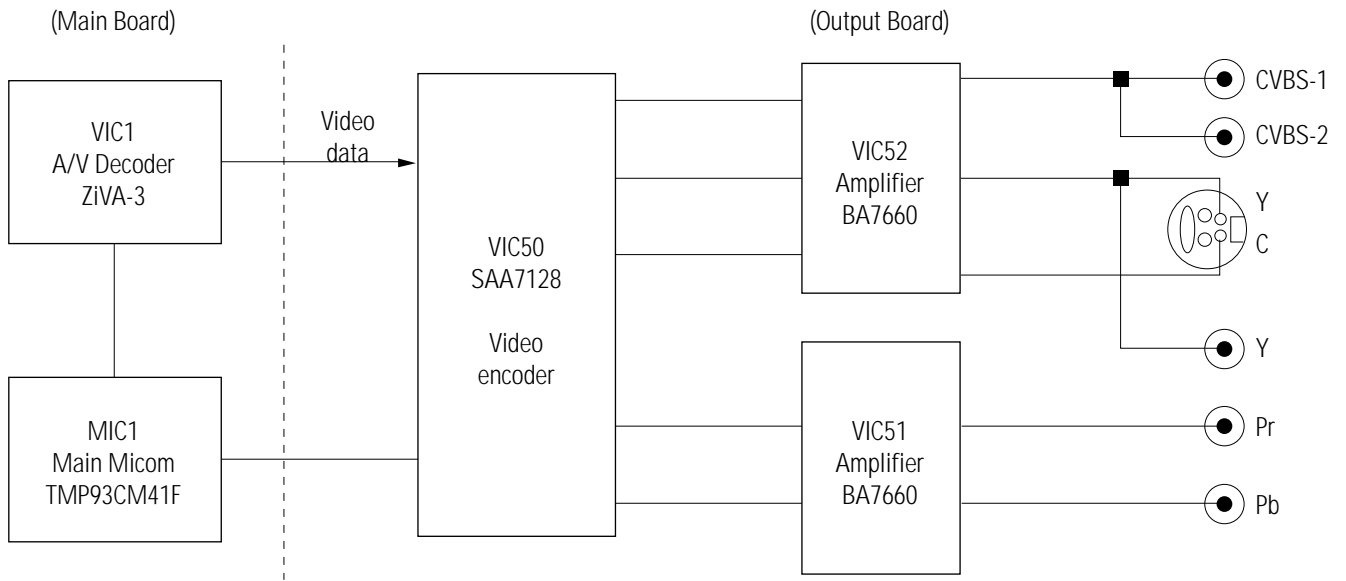


Fig. 6-21 Video Output Block Diagram

6-6-2 NTSC/PAL Digital Encoder (VIC50 : SAA7128)

VIC50 inputted from pin4 with 27MHz generates HSYNC and VSYNC which are based on video signal. Each HSYNC and VSYNC outputted from Pin8 and Pin7 are inputted to Pin157 and Pin158 of A/V decoder VIC1(ZIVA-3). VIC1 is the synchronous signals with the video signal and control the output timing of 8bit video signal of ITU-R601 format. (Pin180, 182, 184 ~ 189 (MSP))

8bit data is inputted to Pin9(MSB) and Pin16 of VIC50 and the inputted data is demuxed with each 8bit of Y/R-Y/B-Y. The separate signal is encoded to NTSC or PAL by control of MIC1. The above signals, that is CVBS (Composite Video Burst Synchronized)(Pin30), S-Video (Y:Pin27, C:Pin24), Y/Pb/Pr(Pin27/Pin29/Pin23) and GB(Pin26/Pin29/Pin23). In course of encoding, 8bit data can extend to 10bit or more. To convert the extended data to quantization noise as possible, VIC50 adopts 10bit D/A converter. VIC50 perform video en-coding as well as copy protection.

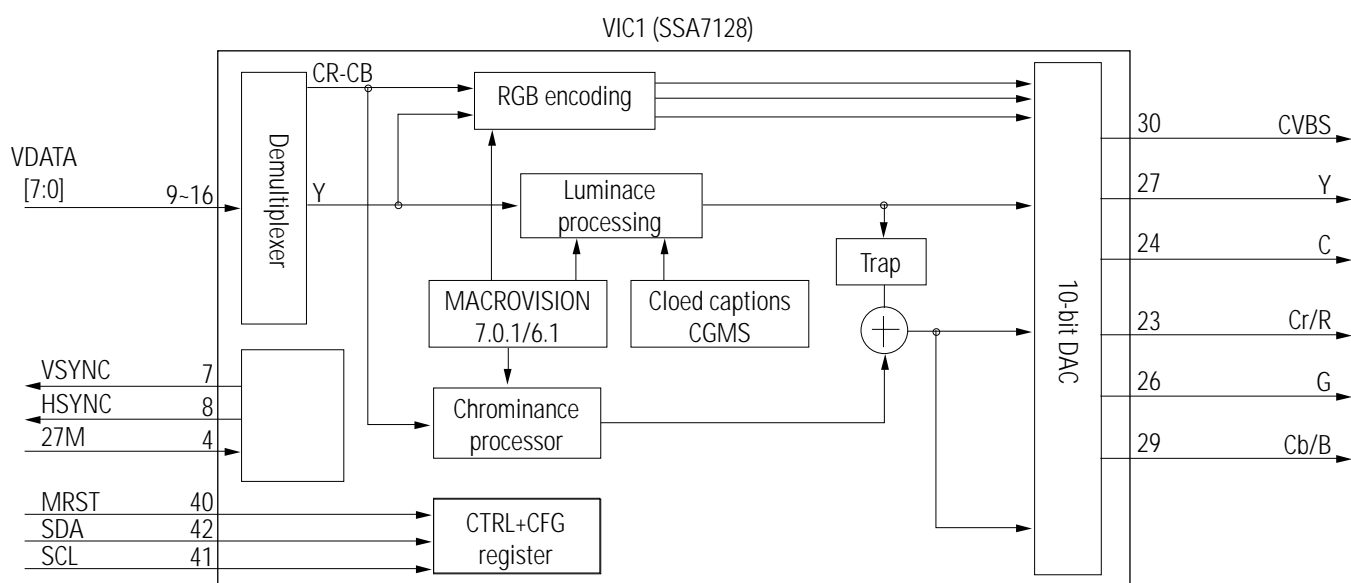


Fig. 6-22

6-6-3 Amplifier (VIC51, VIC52 : BA7660)

VIC51 and VIC52 are 6dB amplifier. Based on CVBS signal, the final output level must be 2Vpp without 75ohm terminal resistance. Because the level of video encoder output is only 1.1Vpp, the level is adjusted with the special amplifier. When mute of pin1 is high active, if the pin is floating and connected to power, the output signal is never outputted. CVBS, Y, C, Cr and Cb outputted from video encoder are inputted to VIC52 (Pin7, Pin2 and Pin4) and VIC51 (Pin7 and Pin4) respectively and outputted from VIC52 (Pin10, Pin15 and Pin13) and VIC51 (Pin10 and Pin 13). Pin9, Pin12 and Pin14 of VIC51 and VIC52 are feedback pin to SAG compensation(DC characteristic compensation of signal). Resistance(VR3-VR14) which is inserted to input terminal is bias resistance for input offset. The signal to which gain is adjusted by amplifier is outputted from jack via 75ohm.

6-6-4 Scart Jack Output

The AV1 of scart jacks is used for connecting a TV or other display devices and the AV2 for a VCR or other players. When the DVD player is turned on, the RGB, CVBS, or S-VIDEO is outputted to AV1 and CVBS to AV2. When the player is turned off, CVBS signal of the TV is inputted and CVBS or RGB of a VCR inputted via AV2 is outputted. In case of AV2, the reverse signal flow to that.

Switching of power on/off is controlled by SCIC1, SCIC2, and SCIC5.

The control signal (Pin 9,10,11) of SCIC1 and SCIC2 is outputted from PIN100 of FIC1 and connected to the signal(Pin 4) inverted by FIC3.

The control signal(Pin 9,10,11) of SCIC5 is also outputted from Pin100 of FIC1 and inverted again by SCQ8.

According to the characteristics that SCART Jack is supplied same pins for the output of CVBS signal and Y signal and for the R signal and C signal, SCIC3 lets the user select two signals in setup menu.

This control signal (Pin 9,10,11) of the switch is outputted from Pin 92 of FIC1.

The signal selected by switch is amplified by SIC4 and SIC6 and outputted through the SCART jack.

The scart jack has the function select signal (Pin 8 of AV1) that the TV can select automatically RF and the external video signal.

SCQ1 to SCQ7 are the circuit to point, FIC1 (Pin100, 94) controls. When the TV aspect ratio is 4/3 or 16/9, it is outputted 4.5 ~ 7V or 9.5 ~ 12V each. But, when the DVD video source is 16/9 and 16/9 wide is selected in setup menu, 4.5 ~ 7V is outputted. Otherwise, 9.5 ~ 12V is outputted.

When the player is turned off, the TV works with function selection by output signal of VCR in relation of SCQ9 and SCQ10.

RGB control signal (Pin 16 of AV1) is outputted that the TV can select between RGB and CVBS.

SCQ11 ~ SCQ14 and SCQ17 are for RGB control and controlled by FIC1 (Pin91).

When the player is turned off, receives VCR input (Pin 37 of AV2) and buffers in this circuit and then outputs to Pin 16 of AV1.

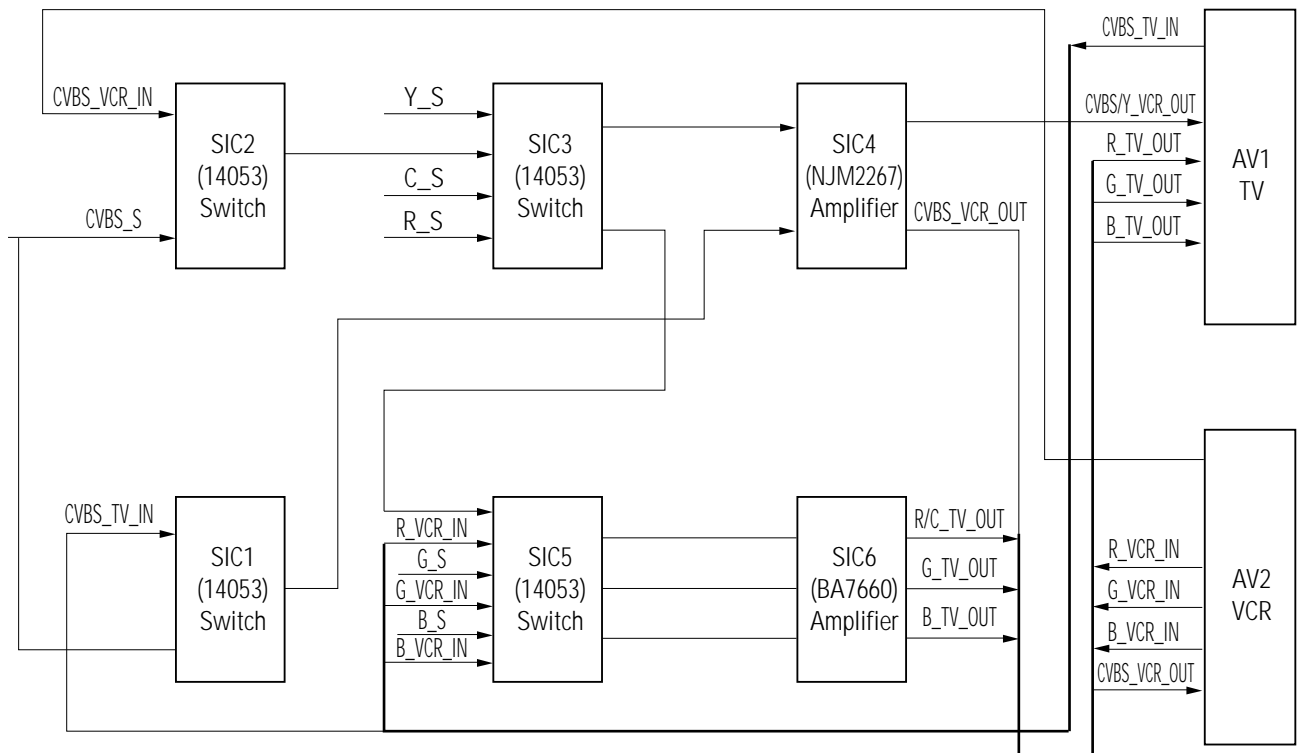


Fig. 6-23

6-7 Audio

6-7-1 Outline

The four data (Data 0~3) outputted from A/V decoder (VIC1 ; ZiVA-3) are supplied to DATA 0 for 2-channel mixed audio output and to DATA 1~3 for Analog audio output (5.1-channel).

The audio data (0~3) transmitted from A/V decoder (VIC1 ; ZiVA-3) are converted into analog signal via audio D/A converter and outputted via post filter and amplifier.

CD and VCD are outputted with only 2 channels audio data and transmit them to Data 0 and Data 1.

Front L/R channel is outputted in mixed audio output (L/R output) and analog audio output and surround L/R, center and subwoofer aren't outputted.

If DVD of 2 channels source disc is used, it is outputted by the same way with CD and VCD.

If 5.1-channel source disc, front L/R channel is outputted in Data 1, Surround L/R in Data 2 and Center/Subwoofer in Data 3. At that time, 5.1 channel can be downmixed in 2 channel in Data 0.

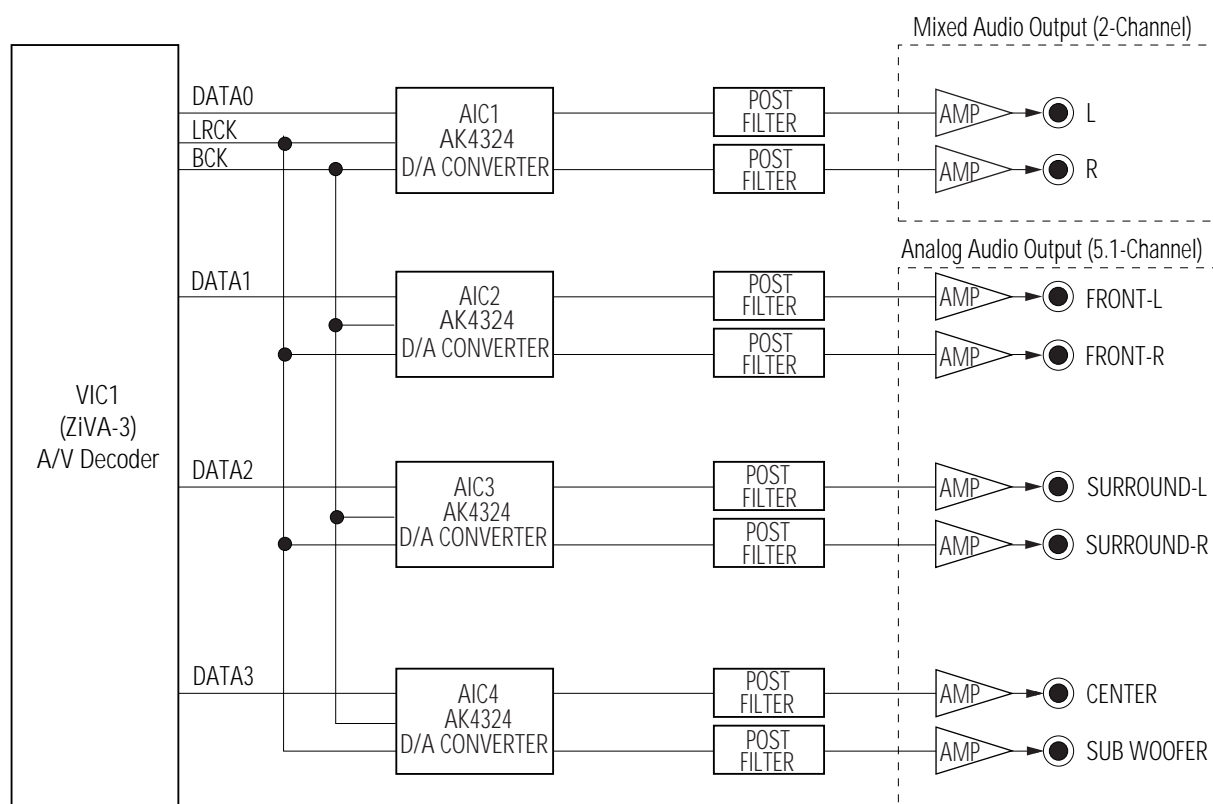


Fig. 6-24 Audio Output Block Diagram

6-7-2 DVD Audio Output

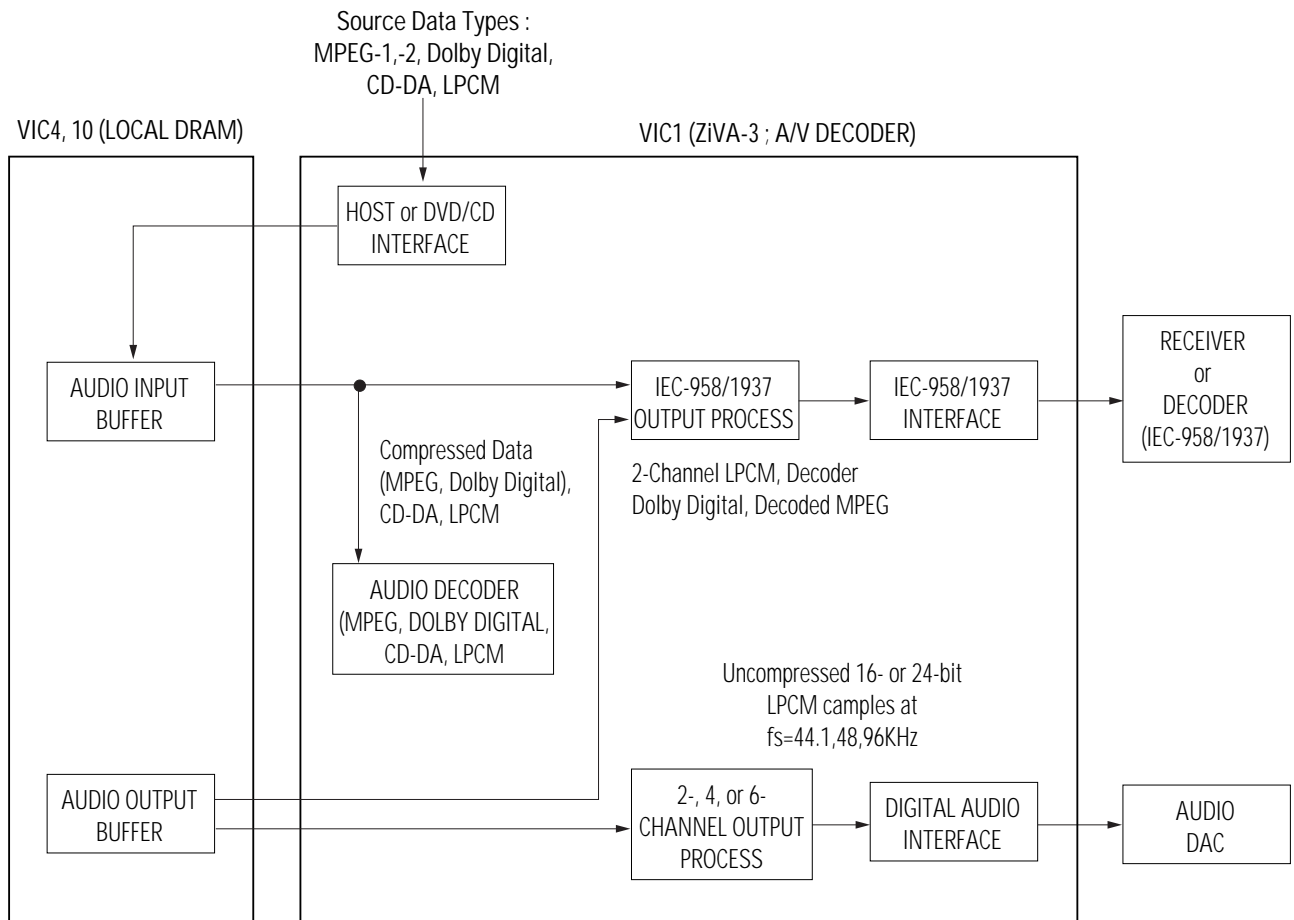


Fig. 6-25 Audio Decoder and Output Interface Datapath

1) Compressed Data

The audio data inputted to VIC1 (ZiVA-3) A/V decoder is divided into compressed data and uncompressed data. It is compressed data that is compressed with multi-channel audio data such as Dolby digital, MPEG, DTS, etc. The compressed data inputted to VIC1 (ZiVA-3) is converted into the uncompressed data of 2, 4, and 6 channels through ZiVA-3 built-in audio decoder and is outputted to Data 0, 1, 2, and 3 through digital audio interface. The compressed data is transmitted to external AC-3 amplifier or MPEG/DTS amplifier as IEC-958/1937 transmission data format compressed by ZiVA-3 built-in IEC-958 output process.

2) Uncompressed Data

The uncompressed data is that data isn't compressed, so it is called CD-DA, LPCM data. The 2 channels data is converted through audio decoder 2-channel data and Data 0 and Data 1 are outputted in digital audio interface. Via IEC-958 output process, they is transmitted to digital amplifier or AC-3/MPEG/DTS amplifier built in the external digital input source with IEC-958/1937 transmission format.