

DATA SHEET



TDA10021 Single Chip DVB-C Channel Receiver

Preliminary specification
File under Integrated Circuits, IC02

2000 March 15

Single Chip DVB-C Channel Receiver

TDA10021

FEATURES

- 4/16/32/64/128/256 QAM demodulator (DVB-C compatible : ETS 300-429).
- High performance for 256 QAM especially for direct IF applications.
- On chip 10-bit ADC.
- On chip PLL for crystal frequency multiplication (Typically 4MHz crystal)
- Digital down conversion.
- Half Nyquist filter (roll off = 15 %).
- Two PWM AGC outputs with programmable take over point (For Tuner and Downconverter Control)
- Clock timing recovery, with programmable second order loop filter.
- Variable symbol rate capability from SACLK/64 to SACLK/4 (SACLK max = 36 MHz)
- Programmable anti-aliasing filters.
- Full digital carrier recovery loop.
- Carrier acquisition range up to 18 % of symbol rate.
- Integrated adaptative equalizer (Linear Transversal Equalizer or Decision Feedback Equalizer).
- On chip FEC decoder (Deinterleaver & RS decoder), full DVB-C compliant.
- DVB compatible differential decoding and mapping.
- Parallel and serial transport stream interface simultaneously .
- I2C bus interface, for easy control.
- CMOS 0.2 μ m technology.

APPLICATIONS

- DVB-C fully compatible.
- Digital data transmission using QAM modulations.
- Cable demodulation.
- Cable modems
- MMDS (ETS 300-429).

DESCRIPTION

The TDA10021 is a single chip DVB-C Channel receiver for 4, 16, 32, 64, 128 and 256-QAM modulated signals. The device interfaces directly to the IF signal, which is sampled by a 10-bit A/D converter.

The TDA10021 performs the clock and the carrier recovery functions. The digital loop filters for both clock and carrier recovery are programmable in order to optimize their characteristics according to the current application.

After base band conversion, equalization filters are used for echo cancellation in cable applications. These filters are configured as T-spaced transversal equalizer or DFE equalizer, so that the system performance can be optimized according to the network characteristics. A proprietary equalization algorithm, independent of carrier offset, is achieved in order to assist carrier recovery. Then a decision directed algorithm takes place, to achieve final equalization convergence.

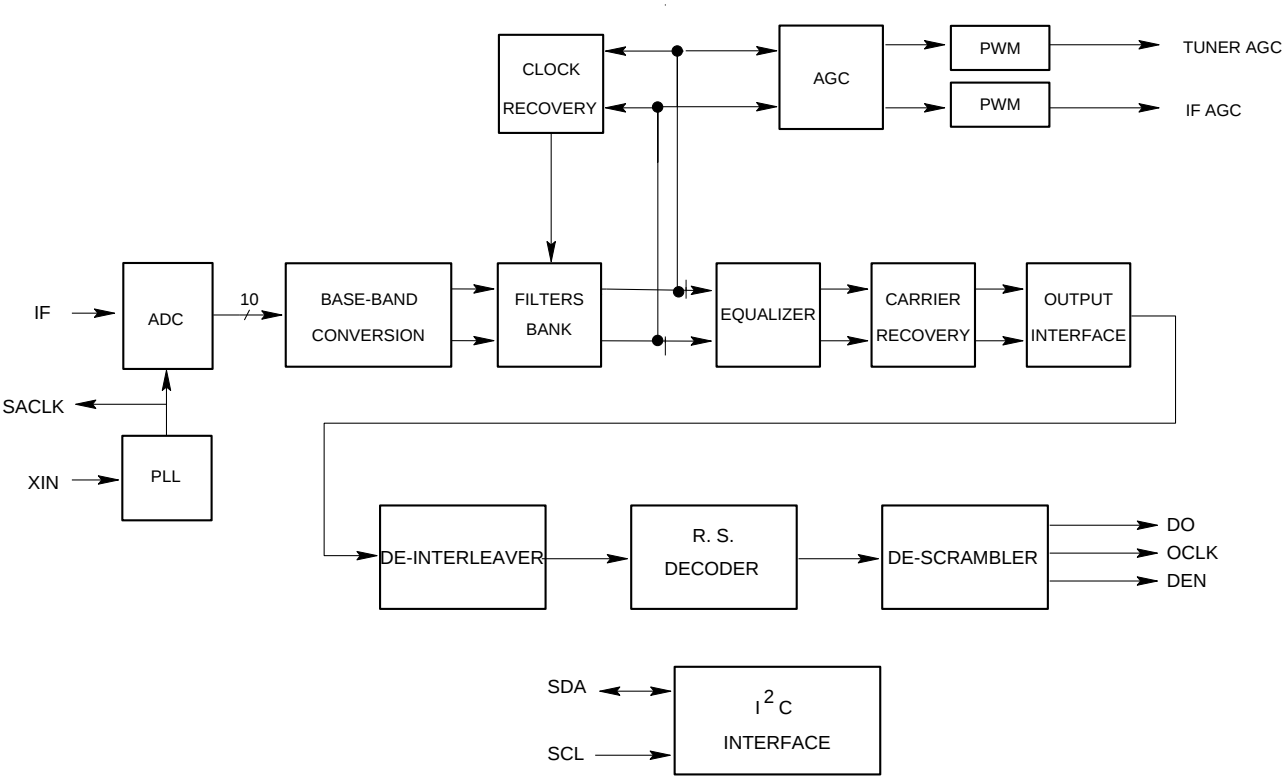
The TDA10021 implements a FORNEY convolutional deinterleaver of depth 12 blocks and a Reed-Solomon decoder which corrects up to 8 erroneous bytes. The deinterleaver and the RS decoder are automatically synchronized thanks to the frame synchronization algorithm which uses the MPEG2 sync byte. Finally descrambling according to DVB-C standard, is achieved at the Reed Solomon output. This device is controlled via an I²C bus.

Designed in 0.2 μ m CMOS technology and housed in a 64 pin TQFP package, the TDA10021 operates over the commercial temperature range.

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FIGURE 1 : FUNCTIONAL BLOCK DIAGRAM



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TABLE 1 : ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Unit
Ambient operating temperature : Ta	0	70	°C
DC supply voltage	- 0.5	Tbd	V
DC Input voltage	- 0.5	VDD + 0.5	V
DC Input Current		± 20	mA
Lead Temperature		+300	°C
Junction Temperature		+150	°C

Stresses above the absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

TABLE 2 : RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VDD	Digital supply voltage	1.62	1.8	1.98	V	1.8V ±10%
VCC	5V supply	4.75	5	5.25	V	pin 13 Only for 5V requirements
Ta	Operating temperature	0		70	°C	Ambient temperature
VIH ¹	High-level input voltage	2		VCC + 0.3	V	TTL input
VIL	Low-level input voltage	-0.5		0.8	V	TTL input
VOH ²	High-level output voltage	VDD -0.1 2.4			V	@ IOH = -0.8 mA @ IOH = + 2mA
VOL ²	Low-level output voltage			0.1 0.4	V	@ IOL = 0.8 mA @ IOL = + 2mA
IDD	Supply current		t.b.d		mA	Fsampl. = 57.84Mhz Symbol Rate =6Mbd
CIN	Input capacitance		t.b.d		pF	
COUT	Output capacitance		t.b.d		pF	
VD1	Analog supply voltage	1.6	1.8	2.0	V	1.8V ± 10%
VD2, VD3	Analog supply voltage	3.0	3.3	3.6	V	3.3V ± 10%
VIP	Positive analog input		0.5		V	
VIM	Negative analog input		-0.5		V	

¹ All inputs are 5V tolerant

² IOH, IOL = ± 4mA only for pins SACLK, OCLK, SDA, CTRL1, CTRL2, IT

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FUNCTIONAL DESCRIPTION➤ **ADC**

The TDA10021 implements a 10-bit analog to digital converter. No external voltage references are required to use the ADC.

➤ **PLL**

The TDA10021 implements a PLL used as clock multiplier by $[M/(N.P)]$ (programmable parameters in index 28₁₆, 29₁₆, 2A₁₆), so that the crystal can be low frequency (fundamental tone – typically 4Mhz)

➤ **DOWN CONVERTER AND NYQUIST FILTERS**

The digital down converter performs the down conversion of the bandpass input signal into the 2 classical quadrature I & Q channels. Then these two signals are passed through anti-alias filters and through a half Nyquist filter having a fixed roll-off of 0.15. The digital filter gives a stop band attenuation of more than 40 dB.

➤ **EQUALIZER**

After Nyquist filtering, the signal is fed to an equalization filter, for echo cancellation. This equalizer can be configured as either a transversal Equalizer or a decision feedback equalizer. The following table shows some echos configuration that the TDA10021 corrects with an equivalent degradation of less than 1dB @ BER = 10^{-4} .

DELAY (nS)	AMPLITUDE (dB)	PHASE
50	-10	worst
150 and 800	-12 and -20	worst
1600	-20	worst

➤ **CARRIER RECOVERY**

The carrier synchronizer implements a fully digital algorithm allowing to recover carrier frequency offsets up to $\pm 18\%$ symbol rate. A phase error detector followed by a programmable second order loop filter provides an estimation of the carrier phase, to compensate the input carrier frequency offset.

➤ **CLOCK RECOVERY**

A timing error detector implements an application of Gardner algorithm for digital clock recovery.

The resulting error is fed to a programmable second order loop filter, which provides a 8-bit command to the NCO block. This one allows to determine the right sampling time instant of the input signal.

➤ **AUTOMATIC GAIN CONTROL (2 PWM outputs)**

An estimation of input signal magnitude is performed and compared to two programmable threshold. The resulting errors are filtered to produce two 10-bit commands which are then PWM encoded and provided on pins VAGC1 and VAGC2. The PWM signals can be passed through two low pass filters to control the gain amplifier.

➤ **OUTPUT INTERFACE**

After carrier recovery, the demodulated output symbol must be decoded according to the constellation diagram given by DVB standard for 4, 16, 32, 64, 128 and 256 QAM. The resulting symbols are then differentially decoded (DVB compliant) and serially provided to the FEC part.

➤ **BLOCK SYNCHRONIZATION**

At demodulator output, the length of some error bursts may exceed that which can be reliably corrected by the Reed-Solomon decoder. The implemented de-interleaving is a convolutional one (Forney) of depth 12. The first operation consists in synchronizing the de-interleaver. This is accomplished by detecting α consecutive MPEG2 sync words (or sync) which are present as the first byte of each packet.

Next, the RAM memory associated with the deinterleaver fills up and the first deinterleaved bytes are provided to the input of the Reed-Solomon decoder. The state machine of the de-interleaver goes to the control phase which

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counts β consecutive missed MPEG2 sync words (or $\overline{\text{sync}}$) before declaring the system desynchronized and going back to the synchronization phase. α and β are programmable through the I2C interface. When the inverted sync word is detected at the input of the de-interleaver, the bytes provided to the Reed-Solomon decoder are inverted at the output of the deinterleaver.

➤ **REED-SOLOMON DECODER**

The Reed-Solomon decoder decodes the symbol stream from the de-interleaver according to the (204, 188) shortened Reed-Solomon code. Synchronization to Reed-Solomon code is defined over the finite Galois field GF(2^8). The field generator polynomial is given by :

$$G(x) = \prod_{i=0}^{15} (x + \alpha^i)$$

This Reed-Solomon decoder corrects up to eight erroneous symbols in each block. When the correction capability of the decoder is exceeded, the block is not changed and is provided as it has been entered. In this case the flag UNCOR is set and the MSB of the second byte in the MPEG2 frame is forced to one (error indicator). The correction capability of the RS decoder can be inhibited.

➤ **DESCRAMBLER**

In order to comply with energy dispersal requirements of radio transmission regulations and to ensure adequate binary transitions, the MPEG2 frames are scrambled at the encoder side. Dual operation is achieved at the output of the Reed-Solomon decoder using the same scrambler/descrambler. The polynomial for the pseudo random binary sequence (PRBS generator is $1 + x^{14} + x^{15}$). The PRBS registers are initialized at the start of every eight transport packets. To provide an initialization signal for the descrambler, the MPEG2 sync byte of the first transport packet is inverted from 47₁₆ to B8₁₆. When detected, the descrambler is loaded with the initial sequence "100101010000000". The descrambler can be inhibited.

➤ **INTERFACE**

The TDA10021 integrates an I²C interface in slave mode. This I2C interface fulfills the Philips component I2C bus specification.

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INPUT - OUTPUT SIGNAL DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
CLR#	16	I (5v tol)	The CLR# input is asynchronous and active low, and clears the TDA10021. When CLR# goes low, the circuit immediately enters its RESET mode and normal operation will resume 4 XIN falling edges later after CLR# returned high. The I2C register contents are all initialized to their default values. The minimum width of CLR# at low level is 4 XIN clock periods.
XIN	2	I	XTAL oscillator input pin. Typically a fundamental XTAL oscillator is connected between the XIN and XOUT pins. The XTAL frequency MUST be chosen so that the system frequency SYSCLK (= XIN * multiplying factor of the PLL) equals to 1.6 times the tuner output Intermediate Frequency : $SYSCLK = 1.6 \times IF$.
XOUT	3	O	XTAL oscillator output pin. Typically a fundamental XTAL oscillator is connected between the XIN and XOUT pins.
SACLK	5	O	Sampling CLock. This output clock can be fed to an external 10-bit ADC as the sampling clock. $SACLK = SYSCLK/2$.
VAGC1	9	O	First PWM encoded output signal for AGC Tuner. This signal is typically fed to the AGC amplifier through a single RC network. The maximum signal frequency on VAGC output is $XIN/16$. AGC information is refreshed every 1024 symbols.
VAGC2	11	O	Second PWM encoded output signal for AGC IF. This signal is typically fed to the AGC amplifier through a single RC network. The maximum signal frequency on VAGC output is $XIN/16$. AGC information is refreshed every 1024 symbols. But VAGC2 can also be configured to output a PWM signal, which value can be programmed through the I2C interface (see register PWMREF, index 34 ₁₆).
DO[7:0]	37,38,39,40 45,46,47,48	O	Data Output bus . These 8-bit parallel data are the outputs of the TDA10021 after demodulation, de-interleaving, RS decoding and de-scrambling. When one of the two possible parallel interfaces is selected (Parameter SERINT=0, index 20 ₁₆) then DO[7:0] is the transport stream output. When the serial interface is selected (Parameter SERINT=1, index 20 ₁₆) then the serial output is on pin DO[0] (pin 48).
OCLK	35	O	Output CLock. OCLK is the output clock for the parallel DO[7:0] outputs. OCLK is internally generated depending on which interface is selected.
DEN	36	O	Data ENable : this output signal is high when there is a valid data on output bus DO[7:0].
UNCOR	33	O	UNCORrectable packet. This output signal is high when the provided packet is uncorrectable (during the 188 bytes of the packet). The uncorrectable packet is not affected by the Reed Solomon decoder, but the MSB of the byte following the sync. byte is forced « 1 » for the MPEG2 process : Error Flag Indicator (if RSI and IEI are set low in the I2C table).
PSYNC	34	O	Pulse SYNChro. This output signal goes high when the sync byte (47 ₁₆) is provided, then it goes low until the next sync byte. If the serial interface is selected, then PSYNC is high only during the first bit of the sync byte (47 ₁₆).
IICDIV	10	I (5v tol)	IICDIV allow to select the frequency of the I2C internal system clock, depending on the crystal frequency. Internal I2C clock is a division of XIN by 4^{IICDIV} and must be between 6 and 20 MHz.

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SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
SADDR	12	I (5v tol)	SADDR is the LSB of the I2C address of the TDA10021. The MSBs are internally set to 000110. Therefore the complete I2C address of the TDA10021 is (MSB to LSB) : 0, 0, 0, 1, 1, 0, SADDR.
SDA	18	I/O (5v tol)	SDA is a bidirectional signal. It is the serial input/output of the I2C internal block. A pull-up resistor (typically 4.7 kΩ) must be connected between SDA and VDD for proper operation (Open Drain output).
SCL	17	I (5v tol)	I2C clock input. SCL should nominally be a square wave with a maximum frequency of 400KHz. SCL is generated by the system I2C master.
TEST	6	I (5v tol)	Test input pin. For normal operation of the TDA10021, TEST must be grounded.
ENSERI	21	I (5v tol)	When high this pin enables the serial output transport stream through the boundary scan pins (TRST,TDO,TCK,TDI,TMS). Must be set low in bist and boundary scan mode.
TRST	26	I/O (5v tol)	Test ReSeT. This active low input signal is used to reset the TAP controller when in boundary scan mode. In normal mode of operation TRST must be set low. <i>In serial mode, TRST is the the uncorrectable output.</i>
TDO	28	O	Test Data Out. This is the serial Test output pin used in boundary scan mode. Serial Data are provided on the falling edge of TCK. <i>In Serial mode, TDO is the data output.</i>
TCK	22	I/O (5v tol)	Test Clock : an independant clock used to drive the TAP controller when in boundary scan mode. In normal mode of operation, TCK must be set low. <i>In serial mode, TCK is the clock output.</i>
TDI	23	I/O (5v tol)	Test Data In. The serial input for Test data and instruction when in boundary scan mode. In normal mode of operation, TDI must be set to low. <i>In serial mode, the TDI is the psync output.</i>
TMS	27	I/O (5v tol)	Test Mode Select. This input signal provides the logic levels needed to change the TAP controller from state to state. In normal mode of operation, TMS must be set to high. <i>In serial mode TMS is then den output.</i>
CTRL	32	O	CTRL is a control output pin programmable by I2C (parameter CTRL of register CONTROL (index 2C ₁₆)). CTRL is open drain output, and therefore requires an external pull up resistor.
SCLT	20	O	SCLT can be configured to be a control line output or to output SCL input. This is controlled by parameter BYPIIC and CTRL_SCLT of register TEST (index 0F ₁₆). SCLT is an open drain output and therefore requires an external pull up resistor.
SDAT	19	I/O (5v tol)	SDAT is equivalent to SDA I/O of TDA10021 but can be tri-stated by I2C programming. It is actually the output of a switch controlled by parameter BYPIIC of register TEST (index 0F ₁₆). SDAT is an open drain output and therefore requires an external pull up resistor.
GPIO	29	O	GPIO can be configured by I2C (parameter selgpio[1:0], index 0F ₁₆) either as: - a front end lock indicator (FEL) (default mode), or - an active low output interrupt line (IT) which can be configured by the I2C interface. See registers ITsel (index 32 ₁₆) and Itstat (index 33 ₁₆), or - a control output pin programmable by I2C (parameter CTRL_GPIO, index 2C ₁₆). GPIO is an open drain output and therefore requires an external pull up resistor.

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SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
VIP	58	I	Positive input to the A/D converter. This pin is DC biased to half-supply through an internal resistor divider (2 x 20kΩ resistors). In order to stay in the range of the ADC, VIP-VIM should remain between the input range corresponding to the sw0 and sw1 bits (index 1B ₁₆ - default value = 0.5 v).
VIM	57	I	Negative input to the A/D converter. This pin is DC biased to half-supply through an internal resistor divider (2 x 20kΩ resistors). In order to stay in the range of the ADC, VIP-VIM should remain between the input range corresponding to the sw0 and sw1 bits (index 1B ₁₆ - default value = 0.5 v).
VREFP	53	O	This is a positive voltage reference for the A/D converter. It is derived from the internal bandgap voltage, VBG, with an on-chip fully differential amplifier.
VREFM	54	O	This is the negative voltage reference for the A/D converter. It is derived from the internal bandgap voltage, VBG, with an on-chip fully differential amplifier.
VD1	50	I	Power supply input for the digital switching circuitry (1.8 typ).
VS1	49	I	Ground return for the digital switching circuitry.
VD2	52	I	Power supply input for the analog clock drivers (3.3V typ).
VS2	51	I	Ground return for the analog clock drivers.
VD3	60,55	I	Power supply input for the analog circuits (3.3V typ).
VS3	59,56	I	Ground return for analog circuits.
DVCC	61	I	1.8V supply for the digital section of the PLL.
DGND	62	I	Ground connection for the digital section of the PLL.
PLLGND	63	I	Ground connection for the analog section of the PLL.
PLLVCC	64	I	3.3V supply for the analog section of the PLL.

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FIGURE 2 : BLOCK DIAGRAM

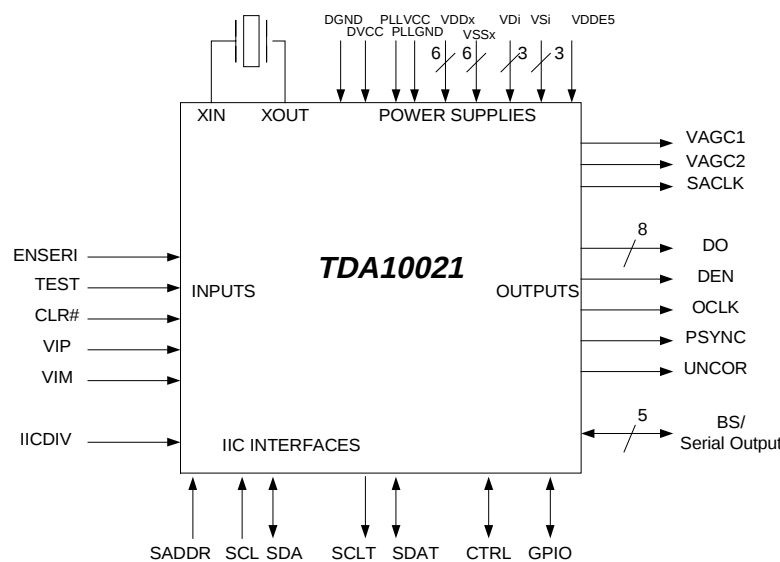
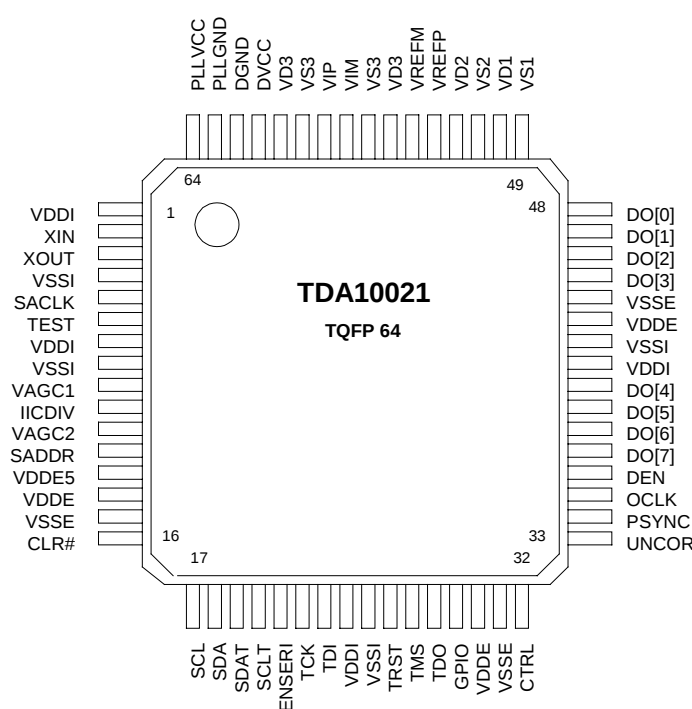


FIGURE 3 : PIN CONFIGURATION



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TABLE 3 : PIN DESCRIPTION

Pin	Pin Name	Direction
1	VDDI	-
2	XIN	I
3	XOUT	O
4	VSSI	-
5	SACLK	O
6	TEST	I
7	VDDI	-
8	VSSI	-
9	VAGC1	OD
10	IICDIV	I
11	VAGC2	OD
12	SADDR	I
13	VDDE5	-
14	VDDE	I
15	VSSE	I
16	CLR#	I
17	SCL	I
18	SDA	I/OD
19	SDAT	I/OD
20	SCLT	I/OD
21	ENSERI	I
22	TCK	I/O
23	TDI	I/O
24	VDDI	-
25	VSSI	-
26	TRST	I/O
27	TMS	I/O
28	TDO	O
29	GPIO	OD
30	VDDE	-
31	VSSE	-
32	CTRL	OD
33	UNCOR	O

Pin	Pin Name	Direction
34	PSYNC	O
35	OCLK	O
36	DEN	O
37	DO[7]	O
38	DO[6]	O
39	DO[5]	O
40	DO[4]	O
41	VDDI	-
42	VSSI	-
43	VDDE	-
44	VSSE	-
45	DO[3]	O
46	DO[2]	O
47	DO[1]	O
48	DO[0]	O
49	VS1	-
50	VD1	-
51	VS2	-
52	VD2	-
53	VREFP	-
54	VREFM	-
55	VD3	-
56	VS3	-
57	VIM	-
58	VIP	-
59	VS3	-
60	VD3	-
61	DVCC	-
62	DGND	-
63	PLLGND[5]	-
64	PLLVCC	-

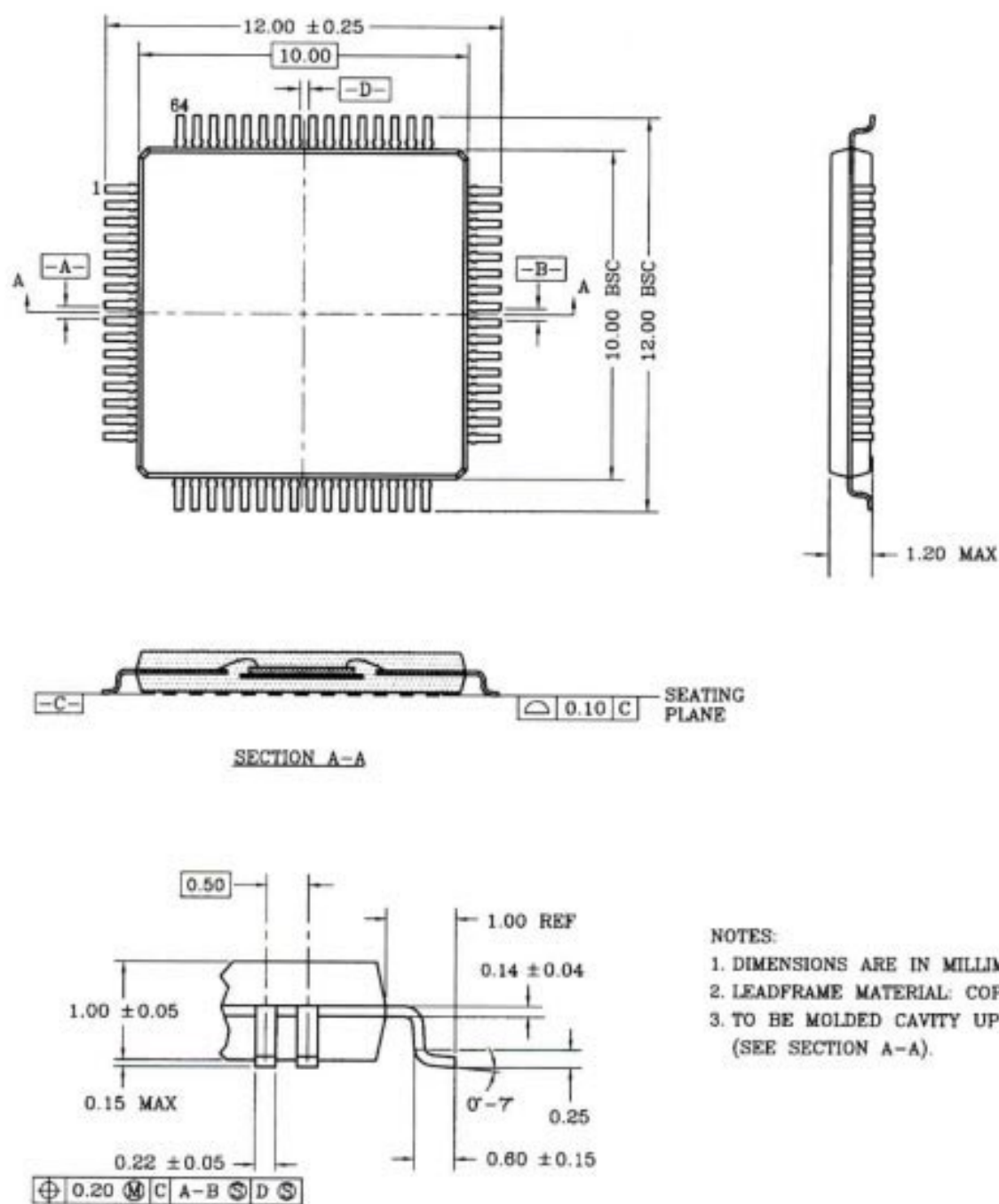
Notes :

1.All inputs (I) are TTL, 5V tolerant inputs

2.OD are Open Drain 5V outputs, so they must be connected to a pull-up resistor to either VDD or VCC

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PACKAGE DESCRIPTION

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DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS ⁽¹⁾
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device.

These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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NOTES

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NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 3 Figtree Drive, HOMEBUSH, NSW 2140,
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),
Tel. +39 039 203 6838, Fax +39 039 203 6800

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Al.Jerozolimskie 195 B, 02-222 WARSAW,
Tel. +48 22 5710 000, Fax. +48 22 5710 001

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,
Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 5F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2451, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
60/14 MOO 11, Bangna Trad Road KM. 3, Bagna, BANGKOK 10260,
Tel. +66 2 361 7910, Fax. +66 2 398 3447

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 3341 299, Fax. +381 11 3342 553

For all other countries apply to: Philips Semiconductors,
Marketing Communications, Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN,
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Internet: <http://www.semiconductors.philips.com>

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