NXP DVB-C/MCNS channel receiver TDA10023HT

Cable demodulators suitable for all countries worldwide

Featuring a high performance QAM demodulator, 10-bit ADC and FEC decoder, the single chip TDA10023HT cable channel receiver provides full compatibility with both DVB-C and MCNS standards, and is suitable for use in the USA, Korea and Japan and all other countries worldwide.

Applications

- Cable set-top boxes and NIMs
- Personal Video Recorder (PVR) for digital cable
- Integrated Digital TV (iDTV)
- Digital TV PCI card for PC

Key features

- Fully compliant DVB-C (Annex A and C) and MCNS (Annex B) decoders
- Multiple TS JQAM Filter
- 4/16/32/64/128/256 QAM demodulator
- High performance for 256 QAM for direct IF applications
- On chip 10-bit ADC and PLL for crystal frequency multiplication
- Digital filtering embedded to interface seamlessly with the TDA827x Silicon tuner family
- Carrier recovery acquisition range +/- 15 % of symbol rate
- Clock recovery acquisition range up to + 12 %
- Auto-scan compatible (software to be developed)
- Double AGC loop structure with programmable take over points
- Automatic Nyquist filter gain setting
- 26 taps integrated adaptive equalizer (Transversal or DFE)
- Simultaneous parallel and serial transport stream outputs
- Works with a low frequency crystal: typically 16 MHz or lower
- CMOS 0.16 µm / 1.8 V (core) & 3.3 V (periphery) technology
- TQFP 64 package (10x10 mm) fully pin-to-pin compatible with the former TDA10021

The TDA10023HT is a single chip cable channel receiver for 4, 16, 32, 64, 128 and 256-QAM modulated signals. It interfaces directly to the IF signal, which is sampled by a 10-bit analog-to-digital converter.The chip performs both clock and carrier recovery functions, with programmable digital loop filters allowing their characteristics to be optimized according to the current application.

Following baseband conversion, equalization filters perform echo cancellation in either a T-spaced transversal or DFE configuration to provide optimized performance according to network characteristics.A proprietary equalization algorithm, independent of carrier offset, assists carrier recovery while a decision directed algorithm ensures final equalization convergence.

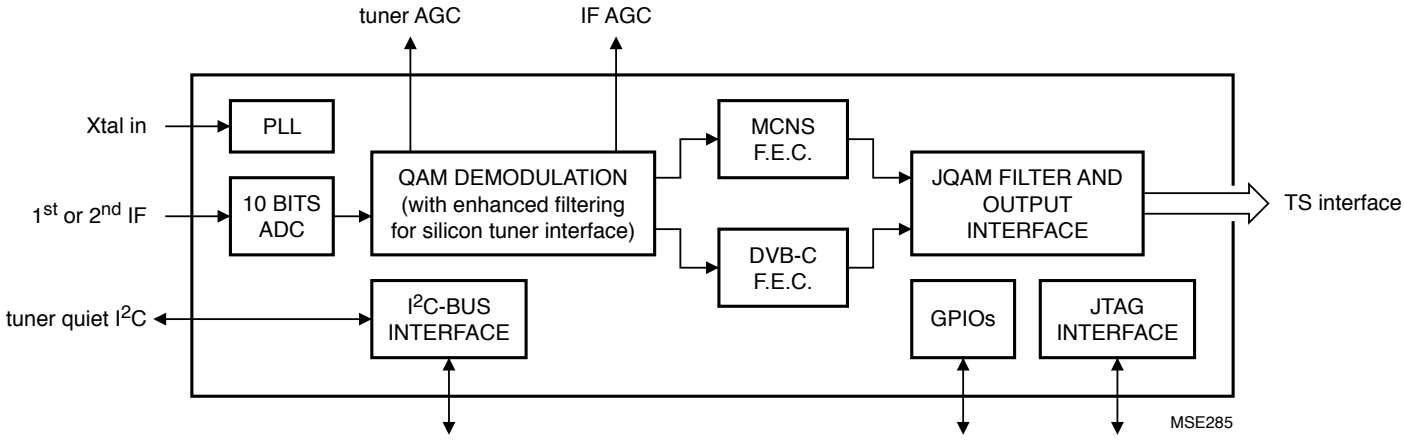
NXP founded by Philips

The chip includes two FEC decoders, one for each standard. In DVB-C mode, a frame synchronization algorithm using the MPEG-2 sync byte automatically synchronizes the 12 block deep FORNEY convolutional deinterleaver and a Reed-Solomon decoder, which can correct up to 8 erroneous bytes.

In MCNS mode, receiver error correction is implemented using a soft decision Trellis decoder (Viterbi) to correct random channel errors, plus a randomizer, a convolutional deinterleaver of depth I=128/64/32/16/8 and J=1/2/3/4/8/16 for burst protection, and a Reed-Solomon decoder which corrects up to 3 erroneous symbols.The deinterleaver and the RS decoder are automatically synchronized using the frame sync trailer.

The TDA10023HT is housed in a 64-pin TQFP package and operates over an extended commercial temperature range (-10 to 70 ˚C).

Evaluation boards are available either with conventional metal can tuners or with the TDA827xA silicon tuner family. An evaluation board comes with all the necessary softwares and PC Graphical User Interface to allow an easy evaluation and development.



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